

74LV574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 04 — 14 May 2009

Product data sheet

1. General description

The 74LV574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops. It is a low-voltage Si-gate CMOS device and is pin and functionally compatible with the 74HC574 and 74HCT574.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW to HIGH CP transition.

When \overline{OE} is LOW, the contents of the eight flip-flops is available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Common 3-state output enable input
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV574N	-40 °C to $+125$ °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV574D	-40 °C to $+125$ °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV574DB	-40 °C to $+125$ °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV574PW	-40 °C to $+125$ °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

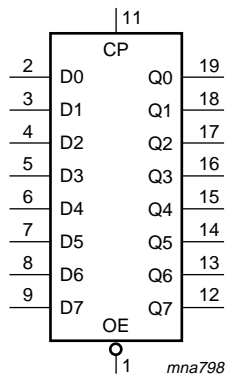


Fig 1. Logic symbol

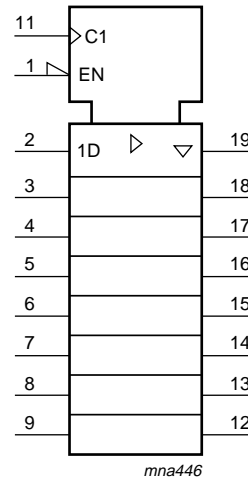


Fig 2. IEC logic symbol

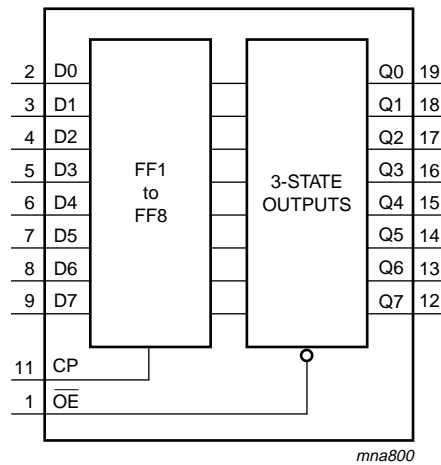


Fig 3. Functional diagram

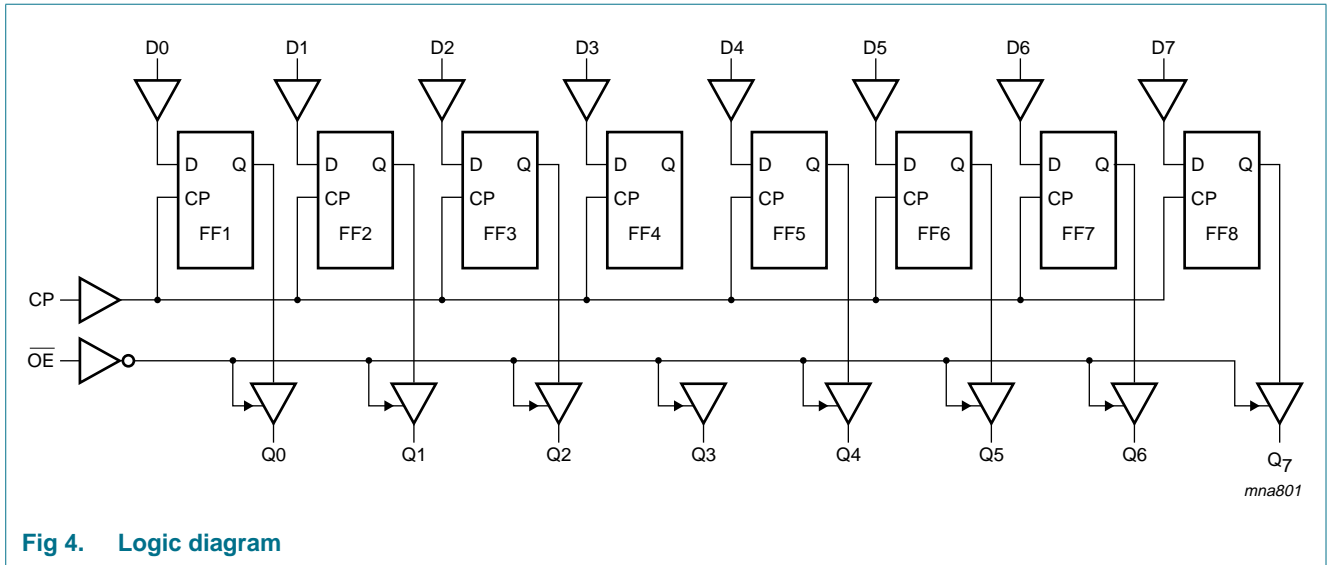


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

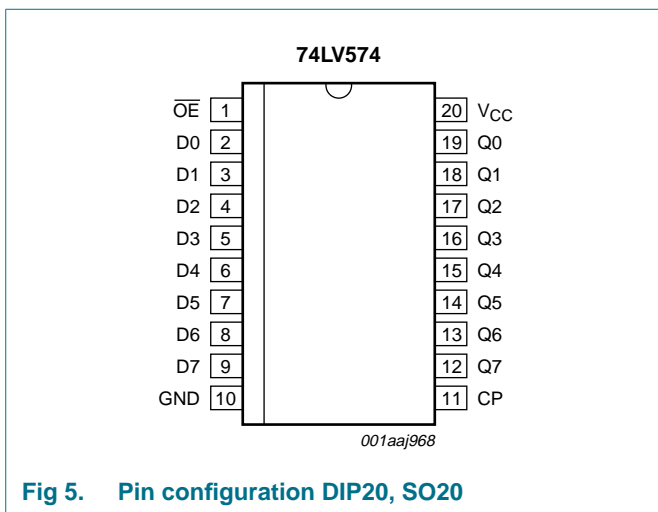


Fig 5. Pin configuration DIP20, SO20

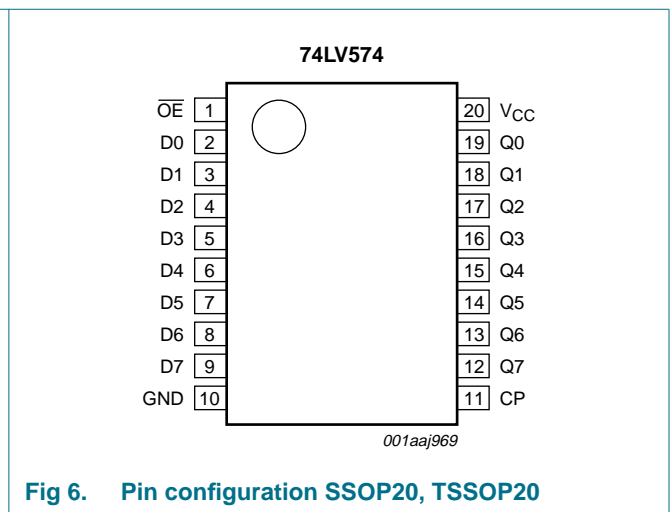


Fig 6. Pin configuration SSOP20, TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
D0 to D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
CP	11	clock input (LOW to HIGH; edge triggered)
Q0 to Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating mode	Input			Internal flip-flop	Output Qn
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition
 Z = high-impedance OFF-state
 ↑ = LOW to HIGH clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	±50	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]		
		DIP20	-	750	mW
		SO20, SSOP20 and TSSOP20	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
 For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage ^[1]		1.0	3.3	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = -100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = -100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = -100 μA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I _O = -100 μA; V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I _O = -8 mA; V _{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
I _O = -16 mA; V _{CC} = 4.5 V	3.6	4.2	-	3.5	-	V		

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I _O = 8 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I _O = 16 mA; V _{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	5	-	10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	-	160	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	CP to Qn; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	80	-	-	-	ns
		V _{CC} = 2.0 V	-	27	34	-	43	ns
		V _{CC} = 2.7 V	-	20	25	-	31	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	13	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	15	20	-	25	ns
		V _{CC} = 4.5 V to 5.5 V	-	-	17	-	21	ns
t _{en}	enable time	OE to Qn; see Figure 8 ^[4]						
		V _{CC} = 1.2 V	-	70	-	-	-	ns
		V _{CC} = 2.0 V	-	24	34	-	43	ns
		V _{CC} = 2.7 V	-	18	25	-	31	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	13	20	-	25	ns
		V _{CC} = 4.5 V to 5.5 V	-	-	17	-	21	ns

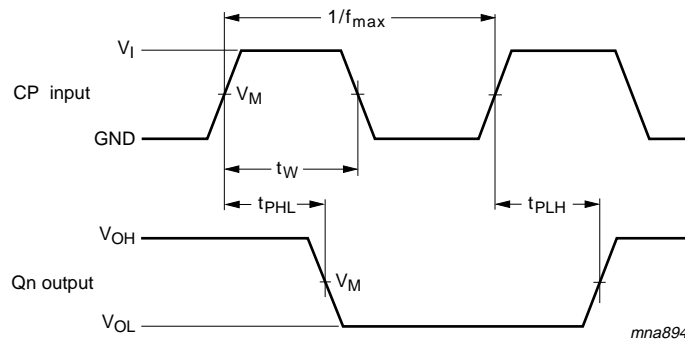
Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{dis}	disable time	OE to Qn; Figure 8 ^[5]						
		V _{CC} = 1.2 V	-	75	-	-	-	ns
		V _{CC} = 2.0 V	-	27	27	-	34	ns
		V _{CC} = 2.7 V	-	21	21	-	26	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	16	17	-	21	ns
t _w	pulse width	CP, HIGH or LOW; see Figure 7						
		V _{CC} = 2.0 V	34	9	-	41	-	ns
		V _{CC} = 2.7 V	25	6	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	20	5	-	24	-	ns
t _{su}	set-up time	Dn to CP; see Figure 9						
		V _{CC} = 1.2 V	-	10	-	-	-	ns
		V _{CC} = 2.0 V	22	4	-	26	-	ns
		V _{CC} = 2.7 V	16	3	-	19	-	ns
t _h	hold time	Dn to CP; see Figure 9						
		V _{CC} = 1.2 V	-	-10	-	-	-	ns
		V _{CC} = 2.0 V	5	-4	-	5	-	ns
		V _{CC} = 2.7 V	5	-3	-	5	-	ns
f _{max}	maximum frequency	see Figure 7						
		V _{CC} = 2.0 V	15	40	-	12	-	MHz
		V _{CC} = 2.7 V	19	58	-	16	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ^[6]		25				pF

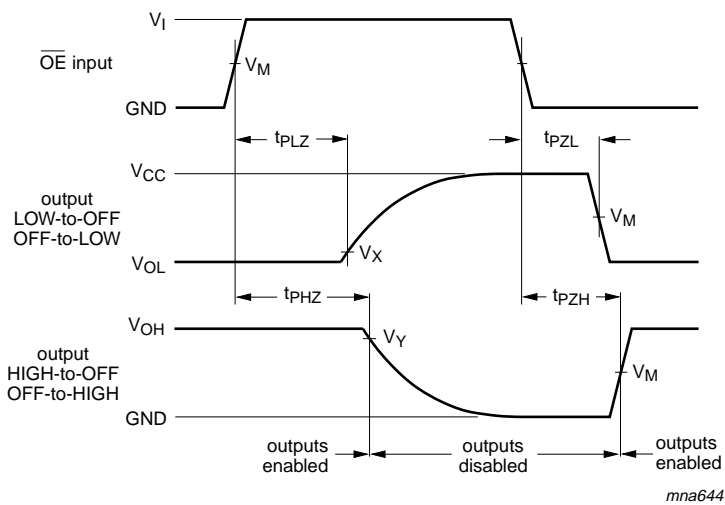
- [1] Typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Typical value measured at V_{CC} = 3.3 V.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



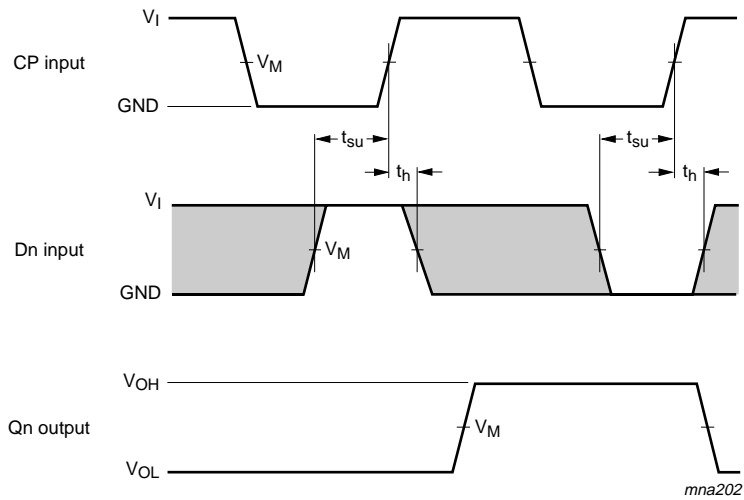
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock (CP) to output (Qn) propagation delays, the clock pulse (CP) and the maximum clock pulse frequency



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Enable and disable times

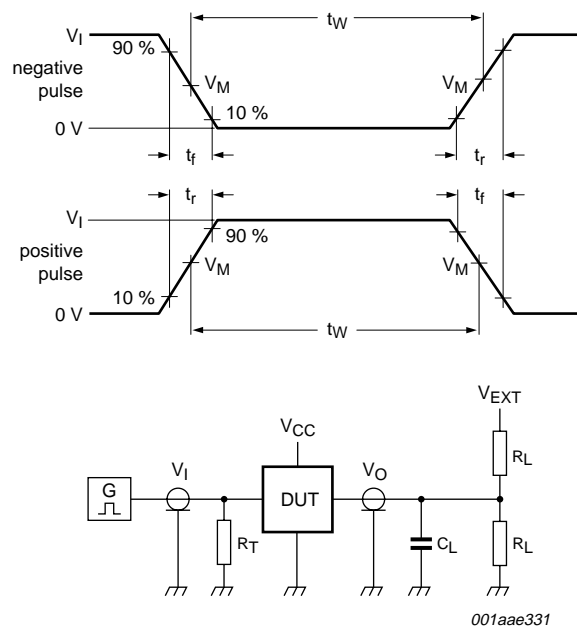


Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. The data set-up and hold times for the Dn input to the CP input)

Table 8. Measurement points

Supply voltage V_{CC}	Input	Output		
	V_M	V_M	V_x	V_y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

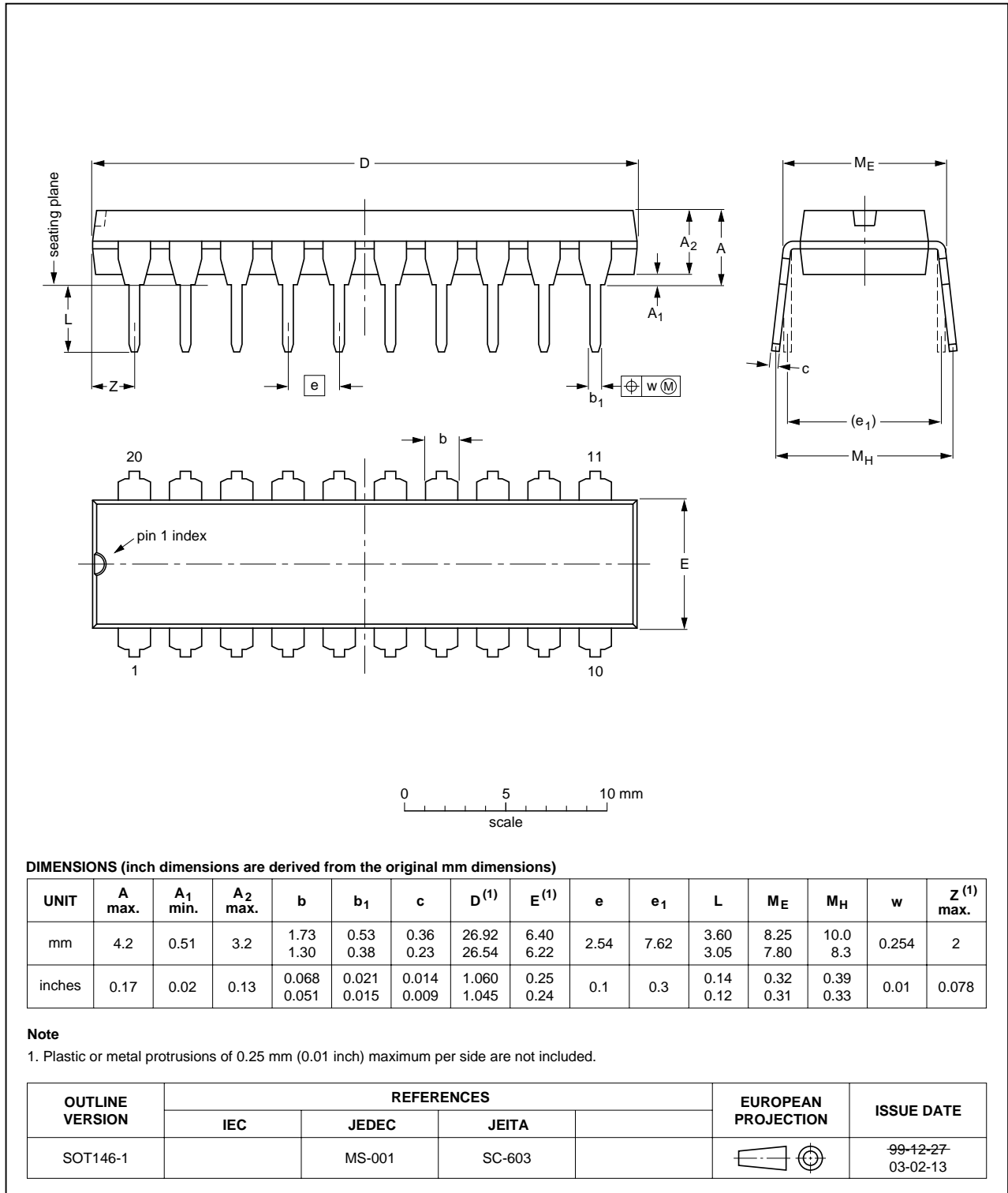


Fig 11. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

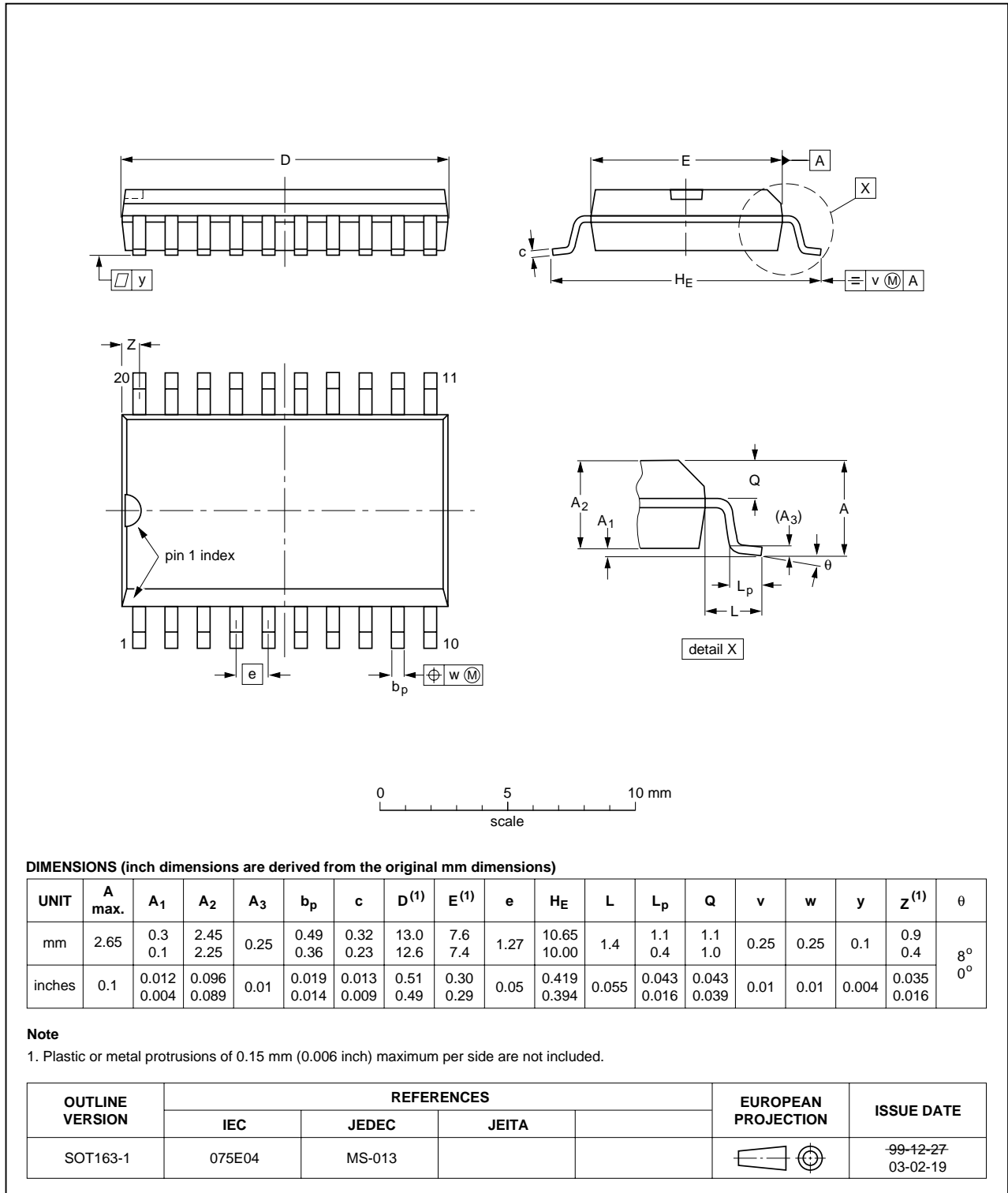


Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

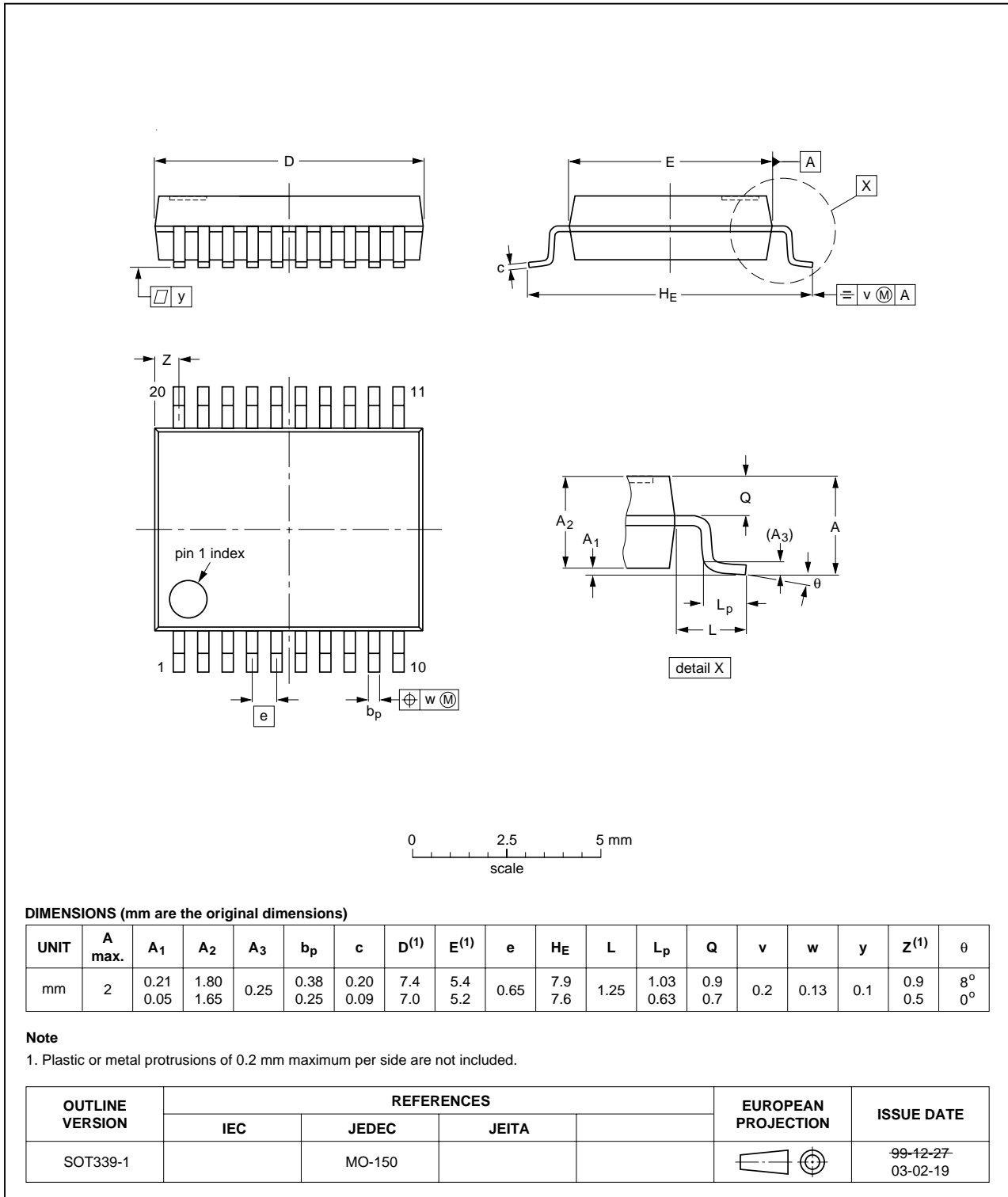


Fig 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

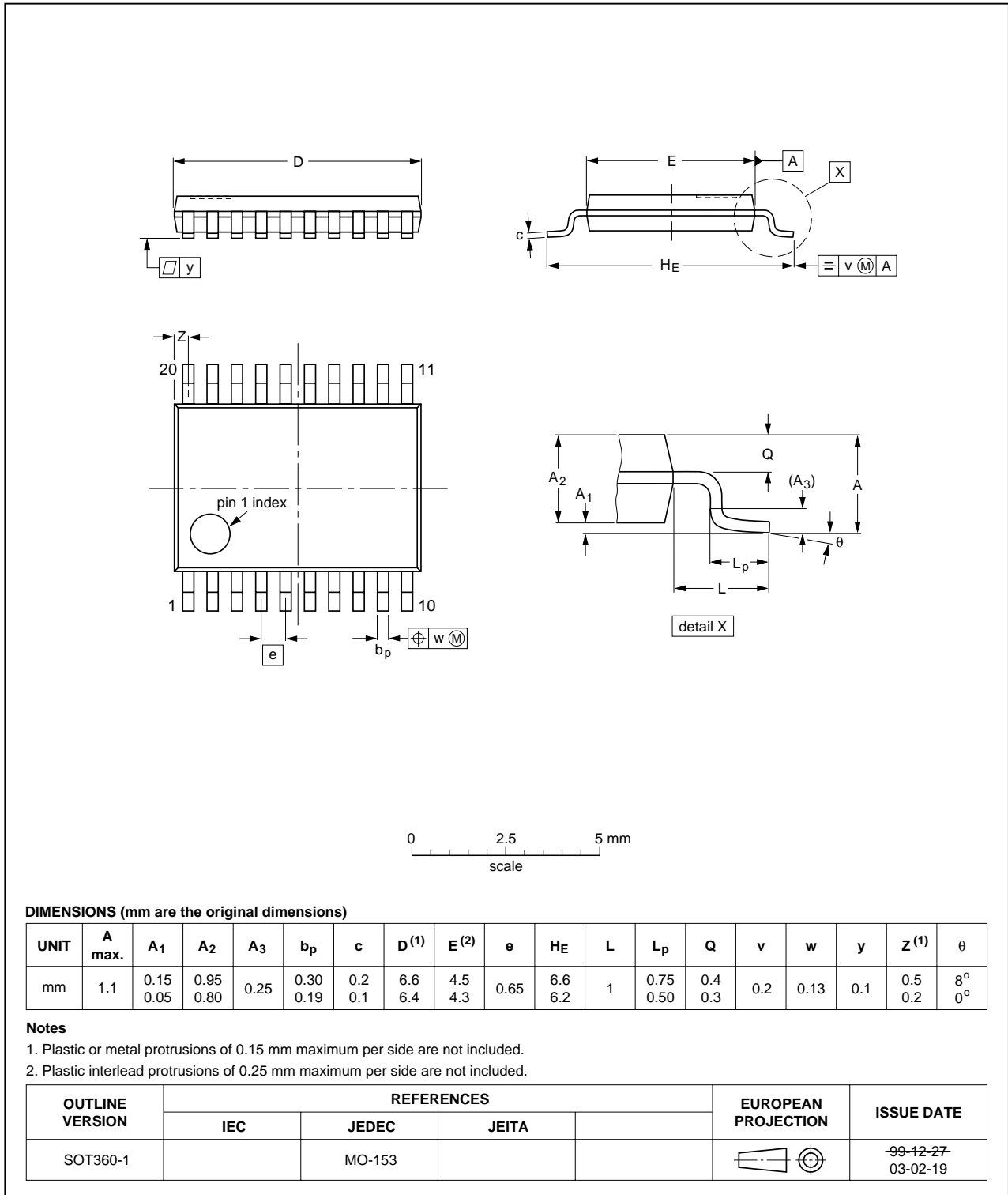


Fig 14. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV574_4	20090514	Product data sheet	-	74LV574_3
Modifications:	• Typo removed from Figure 8 and Table 8 adapted accordingly			
74LV574_3	20090416	Product data sheet	-	74LV574_2
74LV574_2	19970203	Product specification	-	74LV574_1
74LV574_1	19980610	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 14 May 2009

Document identifier: 74LV574_4