PI6CFGL401B

4-Output Low Power PCIE Gen 1-2-3 Clock Generator

Features

- 25MHz crystal or reference clock input
- 100MHz low power HCSL or LVDS compatible outputs
- PCIe 3.0, 2.0 and 1.0 compliant
- Selectable spread spectrum of -0.25%, -0.5% and no spread
- Programmable output amplitude and slew rate
- Cycle-to-cycle jitter (typ.) ~ 30ps
- Supply voltage of 3.3V+/-10%
- Output supply voltage of 1.8V
- Industrial ambient operating temperature
- Available in lead-free package: 32-TQFN

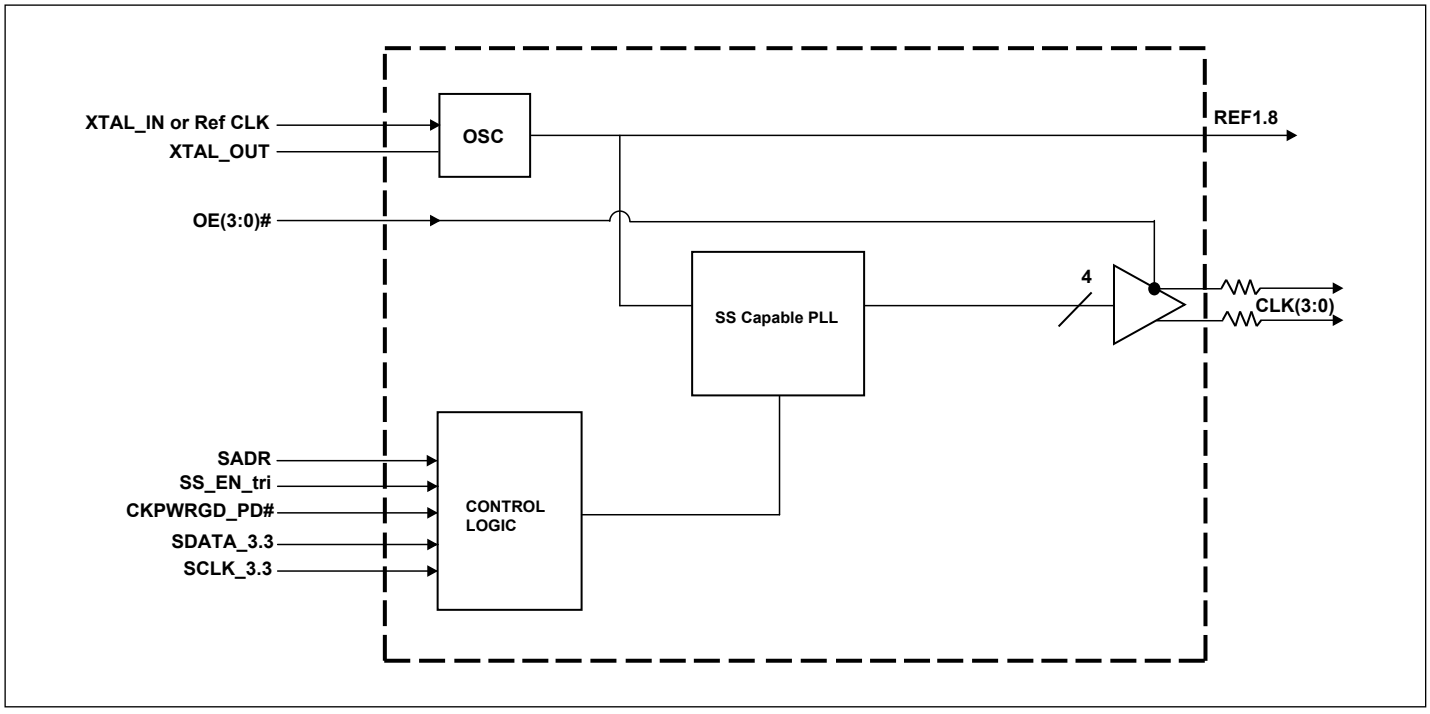
Description

The PI6CFGL401B is an 4-output very low power clock generator for PCIe Gen1-2-3 applications with integrated output terminations providing Zo=100Ω. The device has 4 output enables for clock management and supports 2 different spread spectrum levels in addition to spread off. The device also has one 1.8V LVCMOS REF output.

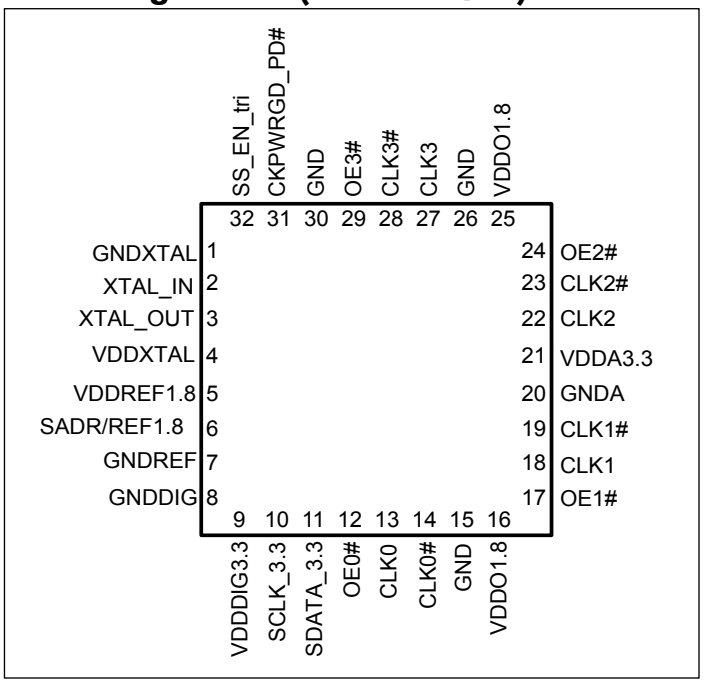
Application

PCIe Gen1-2-3 clock generator

Block Diagram



Pin Configuration (32-Pin TQFN)



SMBus Address Selection Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	1/0
	1	1101010	1/0

Power Connections

Pin Number		Description
VDD	GND	
4	1	XTAL Analog
5	7	REF Output
9	8, 30	Digital Power
16, 25	15, 26	DIF outputs
21	20	PLL Analog

Power Management Table

CKPWRGD_PD#	SMBus OE bit	CLKx		REF1.8
		True O/P	Comp. O/P	
0	x	Low	Low	Hi-Z[1]
1	1	Running	Running	Running
1	0	Low	Low	Low

Note:
1. REF1.8 is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF1.8 is Low.

CKPWRGD_PD#	OE (Pin)	OE (SMBus bit)	CLKx	
			True O/P	Comp. O/P
0	X	x	Low	Low
1	0	0	Low	Low
1	0	1	Running	Running
1	1	0	Low	Low
1	1	1	Low	Low

Pin Description

Pin#	Pin Name	Type	Description
1	GNDXTAL	Power	GND for XTAL
2	XTAL_IN	Input	Crystal input or Reference Clock input. Nominally 25MHz.
3	XTAL_OUT	Output	Crystal output.
4	VDDXTAL	Power	3.3 Power supply for XTAL.
5	VDDREF1.8	Power	VDD for REF output. nominal 1.8V.
6	SADR/REF1.8	Input/Output	Latch to select SMBus Address/1.8V LVCMOS Ref output.
7	GNDREF	Power	Ground pin for the REF outputs.
8	GNDDIG	Power	Ground pin for digital circuitry.
9	VDDDIG3.3	Power	3.3V digital power (dirty power)
10	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	Input/Output	Data pin for SMBus circuitry, 3.3V tolerant.
12	OE0#	Input	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	CLK0	Output	Differential true clock output
14	CLK0#	Output	Differential Complementary clock output
15	GND	Power	Ground pin.
16	VDDO1.8	Power	Power supply for outputs, nominally 1.8V, range 1.05V~3.3V.
17	OE1#	Input	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	CLK1	Output	Differential true clock output
19	CLK1#	Output	Differential Complementary clock output
20	GNDA	Power	Ground pin for the PLL core.
21	VDDA3.3	Power	3.3V power for the PLL core.
22	CLK2	Output	Differential true clock output.
23	CLK2#	Output	Differential Complementary clock output.
24	OE2#	Input	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	VDDO1.8	Power	Power supply for outputs, nominally 1.8V, range 1.05V~3.3V.
26	GND	Power	Ground pin.
27	CLK3	Output	Differential true clock output
28	CLK3#	Output	Differential Complementary clock output
29	OE3#	Input	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
30	GND	Power	Ground pin.
31	CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	SS_EN_tri	Input	Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential	4.6V
All Inputs and Output	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000V(HBM)

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics–Current Consumption

(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
I_{DDAOP}	Operating Supply Current[1]	VDDA3.3, All outputs active @100MHz			40	mA
I_{DDOP}		Total power consumption, All outputs active @100MHz			53	mA
I_{DDSUSP}	Suspend Supply Current[1]	VDDREF1.8, CKPWRGD_PD# = 0, Wake-On-LAN enabled			8	mA
I_{DDPD}	Powerdown Current[1,2]	CKPWRGD_PD#=0			1.3	mA

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Assuming REF is not running in power down state.

Electrical Characteristics–Differential Output Duty Cycle, Jitter, and Skew Characterisitics

(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
t_{DC}	Duty Cycle[1]	Measured differentially, PLL Mode	45		55	%
t_{sk3}	Skew, Output to Output[1]	V_T = 50%			50	ps
$t_{jcyc-cyc}$	Jitter, Cycle to cycle[1]	PLL mode			50	ps

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{DDX}	Supply Voltage[1]	Supply voltage for core, analog	3.0	3.3	3.6	V
V_{DDO}	Supply Voltage[1]	Supply voltage outputs	1.05	1.8	3.3	V
T_A	Ambient Operating Temperature[1]		-40	25	85	°C
V_{IH}	Input High Voltage[1]	Single-ended inputs, except SMBus, SS_EN_tri	0.65 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage[1]	SS_EN_tri	0.4 V_{DD}		0.6 V_{DD}	V
V_{IL}	Input Low Voltage[1]	Single-ended inputs, except SMBus, SS_EN_tri	-0.3		0.35 V_{DD}	V
V_{T+}	Schmitt Trigger Postive Going Threshold Voltage[1]	Single-ended inputs, except SS_EN_tri	0.5 V_{DD}		0.6 V_{DD}	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage[1]	Single-ended inputs, except SS_EN_tri	0.4 V_{DD}		0.5 V_{DD}	V
V_H	Hysteresis Voltage[1]	V_{T+} - V_{T-}	0.05 V_{DD}		0.2 V_{DD}	V
V_{OH}	Output High Voltage[1]	Single-ended outputs, except SMBus. I_{OH} = -2mA	V_{DD} -0.45			V
V_{OL}	Outputt Low Voltage[1]	Single-ended outputs, except SMBus. I_{OL} = -2mA			0.45	V
I_{IN}	Input Current[1]	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD (exclude XTAL_IN pin)	-5		5	uA
I_{INP}		Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA
fin	Input Frequency[1]	XTAL, or XTAL_IN	23	25	26	MHz
Lpin	Pin Inductance[1]				7	nH
C_{IN}	Capacitance[1]	Control Inputs	1.5		5	pF
Cout		Output pin capacitance			6	pF
t_{STAB}	Clock output Stabilization[1, 2]	From V_{DD} Power-Up and after input clock stabilization or de-assertion of CKPWRGD_PD# to 1st clock		0.6	1	ms
f_{MODIN}	Input SS Modulation Frequency[1]	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz
$t_{LATOE\#}$	OE# Latency[1, 3]	CLK start after OE# assertion CLK stop after OE# deassertion	1		3	clocks
t_{DRVPD}	Tdrive_PD#[1, 3]	CLK output enable after CKPWRGD_PD# de-assertion			300	us

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions Cont...

Symbol	Parameters	Condition	Min.	Type	Max.	Units
t_F	Fall time[1, 2]	Control inputs			5	ns
t_R	Rise time[1, 2]	Control inputs			5	ns
V_{ILSMB}	SMBus Input Low Voltage[1]				0.8	V
V_{IHSMB}	SMBus Input High Voltage[1]		2.1		3.6	V
V_{OLSMB}	SMBus Output Low Voltage[1]	@ I_{PULLUP}			0.4	V
I_{PULLUP}	SMBus Sink Current[1]	@ V_{OL}	4			mA
V_{DDSMB}	Nominal Bus Voltage[1]	3.3V bus voltage	2.7		3.6	V
t_{RSMB}	SCLK/SDATA Rise Time[1]	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns
t_{FSMB}	SCLK/SDATA Fall Time[1]	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns
f_{MAXSMB}	SMBus Operating Frequency[1, 5]	Maximum SMBus operating frequency			400	kHz

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing. Input Frequency Capacitance
3. Time from deassertion until outputs are >200 mV
4. The differential input clock must be running for the SMBus to be active

Electrical Characteristics–CLK 0.7V Low Power HCSL Outputs

(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
trf	Slew rate[1, 2, 3]	Scope averaging on 1.5V/ns setting	0.7	1.4	1.9	V/ns
		Scope averaging on 3.0V/ns setting	1.6	2.9	4	V/ns
Δtrf	Slew rate matching[1, 2, 4]	Slew rate matching, Scope averaging on			20	%
V_{OH}	Voltage High[1, 7]	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	550		850	mV
V_{OL}	Voltage Low[1, 7]		-150		150	mV
Vmax	Max Voltage[1]	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV
Vmin	Min Voltage[1]		-300			mV
Vswing	Vswing[1, 2, 7]	Scope averaging off	300			mV
Vcross_abs	Crossing Voltage (abs)[1, 5, 7]	Scope averaging off	250		550	mV
Δ-Vcross	Crossing Voltage (var)[1, 6]	Scope averaging off			140	mV

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
6. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.
7. At default SMBus settings.

Electrical Characteristics–Phase Jitter Parameters

(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	INDUSTRY LIMIT	Units
$t_{jphPCIeG1}$ [1, 2, 3, 5]	Phase Jitter, PCI Express	PCIe Gen 1		30	86	ps (p-p)
$t_{jphPCIeG2}$ [1, 2, 5]		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz		0.5	3	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.2	3.1	ps (rms)
$t_{jphPCIeG3}$ [1, 2, 4, 5]		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.46	1	ps (rms)

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. See http://www.pcisig.com for complete specs.
3. Sample size of at least 100k cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
4. Calculated from Intel-supplied Clock Jitter Tool.
5. Applies to all different outputs.

Electrical Characteristics–REF1.8

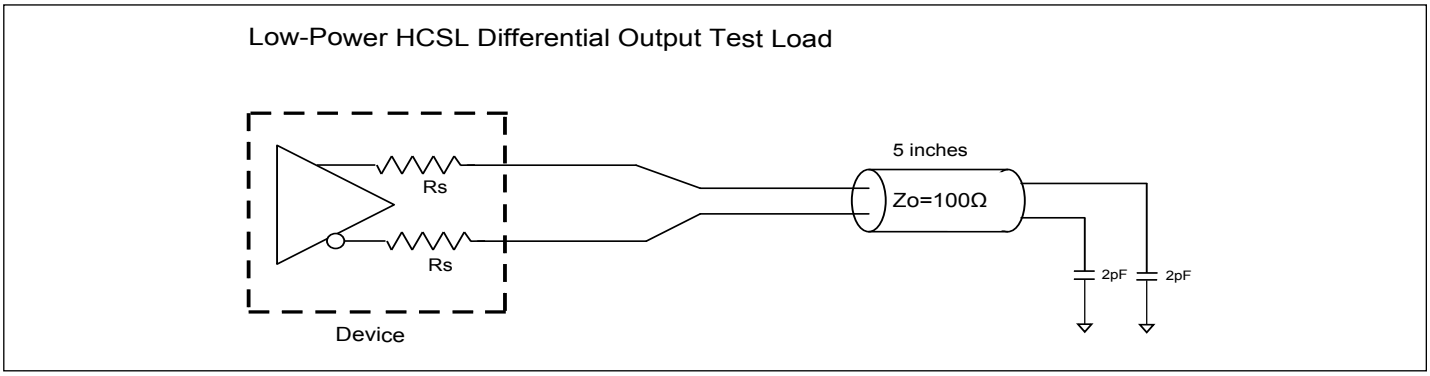
(T_A = -40~85°C; VDD = 3.3V +/- 10%; VDDO = 1.8V +/- 10%, See Test Loads for Loading Conditions)

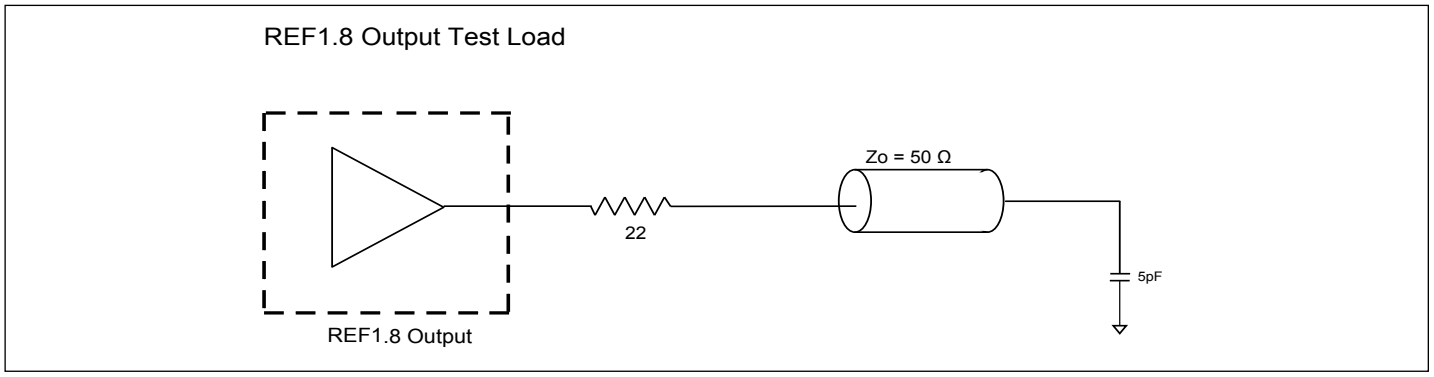
Symbol	Parameters	Condition	Min.	Type	Max.	Units
ppm	Long Accuracy[1, 2]	see Tperiod min-max values		0		ppm
T_{period}	Clock period[1, 2]	25 MHz output nominal		40		ns
t_{rf1}	Rise/Fall Slew Rate[1, 3]	V_{OH} = VDD-0.45V, V_{OL} = 0.45V	0.5		2.5	V/ns
t_{DC}	Duty Cycle[1, 4]	V_T = VDDO/2 V	45		55	%
t_{DCD}	Duty Cycle Distortion[1, 5]	V_T = VDDO/2 V	0		3	%
t_{jc-c}	Jitter, cycle to cycle[1, 4]	V_T = VDDO/2 V			50	ps
t_{jdBc1k}	Noise floor[1, 4]	1kHz offset		-141	-120	dBc
$t_{jdBc10k}$	Noise floor[1, 4]	10kHz offset to Nyquist		-150	-130	dBc
t_{jphREF}	Jitter, phase[1, 4]	12kHz to 5MHz		0.46	1	ps (rms)

Notes:

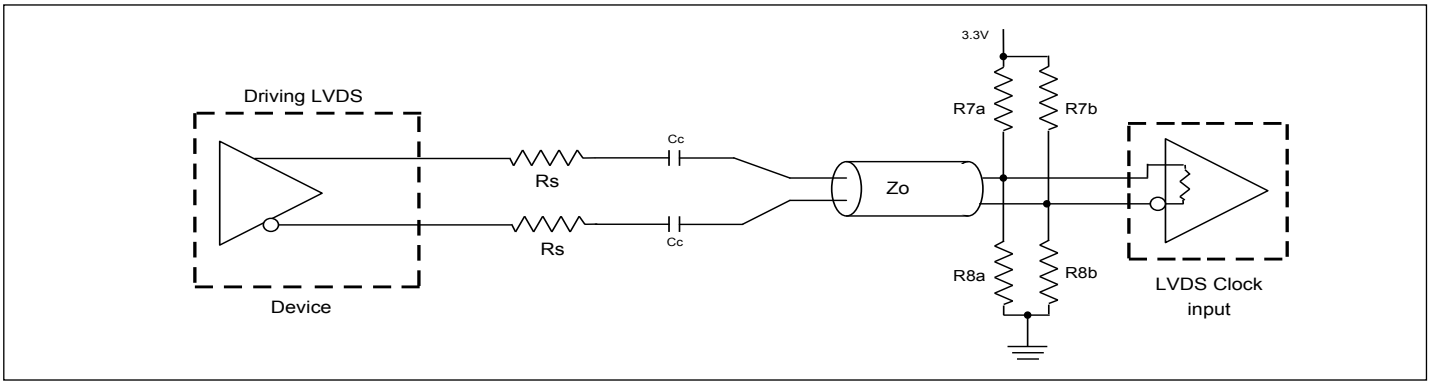
1. Guaranteed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF1.8 is trimmed to 25.00 MHz.
3. Typical value occurs when REF1.8 slew rate is set to default value.
4. When driven by a crystal.
5. When driven by an external oscillator via the XTAL_IN pin. XTALK_OUT should be floating in this case.

Test Loads





Alternate Terminations



Driving LVDS inputs with the PI6CFGL401B

Component	Value	
	Receiver has termination	Receiver does not have termination
R7a, R7b	10K Ω	140 Ω
R8a, R8b	5.6K Ω	75 Ω
Cc	0.1 uF	0.1 uF
Vcm	1.2 volts	1.2 volts

Serial Data Interface (SMBus)

This part is a slave only device that supports blocks read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer by issuing STOP.

Address Assignment

Refer to SMBus Address Selection Table.

Data Protocol

(Write)

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D4	Ack	Register offset	Ack	Byte Count=N	Ack	Data Byte 0	Ack	…	Data Byte N-1	Ack	Stop bit

(Read)

1 bit	8 bits	1	8 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D4	Ack	Register offset	Ack	Repeat start	Slave Addr: D5	Ack	Byte Count=N	Ack	Data Byte 0	Ack	…	Data Byte N-1	NOT Ack	Stop bit

Note:

1.Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

SMBus Table: Output Enable Register

BYTE 0						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	Reserved					1
6	Reserved					1
5	Reserved					1
4	Reserved					1
3	OE3	Output Enable	RW	Low	Enabled	1
2	OE3	Output Enable	RW	Low	Enabled	1
1	OE2	Output Enable	RW	Low	Enabled	1
0	OE0	Output Enable	RW	Low	Enabled	1

SMBus Table: SS Readback and Vhigh Control Register

BYTE 1						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	SSENRB1	SS Enable Readback Bit1	R	00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1'		Latch
6	SSENRB0	SS Enable Readback Bit0	R			Latch
5	SSEN_SWCNTRL	Enable SW control of SS	RW	SS control locked	Values in B1[4:3] control SS amount.	0
4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	00' = SS Off, '01' = -0.25% SS,		0
3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]	'10' = Reserved, '11'= -0.5% SS		0
2	Reserved					1
1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
0	AMPLITUDE 0		RW	10= 0.8V	11 = 0.9V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: CLK Slew Rate Control Register

BYTE 2						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	Reserved					1
6	Reserved					1
5	Reserved					1
4	Reserved					1
3	SLEWRATESEL CLK3	Adjust Slew Rate of CLK3	RW	2.0V/ns	3.0V/ns	1
2	SLEWRATESEL CLK2	Adjust Slew Rate of CLK2	RW	2.0V/ns	3.0V/ns	1
1	SLEWRATESEL CLK1	Adjust Slew Rate of CLK1	RW	2.0V/ns	3.0V/ns	1
0	SLEWRATESEL CLK0	Adjust Slew Rate of CLK0	RW	2.0V/ns	3.0V/ns	1

SMBus Table: REF Control Register

BYTE 3						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	REF 1.8	Slew Rate Control	RW	00 = 0.9V/ns	01 =1.3V/ns	0
6			RW	10 = 1.6V/ns	11 = 1.8V/ns	1
5	REF 1.8 Power Down Function	Wake-on-Lan Enable for REF 1.8	RW	REF 1.8 does not run in Power Down	REF 1.8 runs in Power Down	0
4	REF 1.8 OE	REF 1.8 Output Enable	RW	Low	Enabled	1
3	Reserved					1
2	Reserved					1
1	Reserved					1
0	Reserved					1

Byte 4 is reserved and reads back 'hFF'.

SMBus Table: Revision and Vendor ID Register

BYTE 5						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	RID3	Revision ID	R	A rev = 0000		0
6	RID2		R			0
5	RID1		R			0
4	RID0		R			0
3	VID3	VENDOR ID	R			0
2	VID2		R			0
1	VID1		R			0
0	VID0		R			0

SMBus Table: Device Type/Device ID

BYTE 6						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	Device Type1	Device Type	R	00 = FGV, 01 = DBV,		0
6	Device Type0		R	10 = DMV, 11= Reserved		0
5	Device ID5	Device ID	R	000100 binary or 04 hex		0
4	Device ID4		R			0
3	Device ID3		R			0
2	Device ID2		R			1
1	Device ID1		R			0
0	Device ID0		R			0

SMBus Table: Byte Count Register

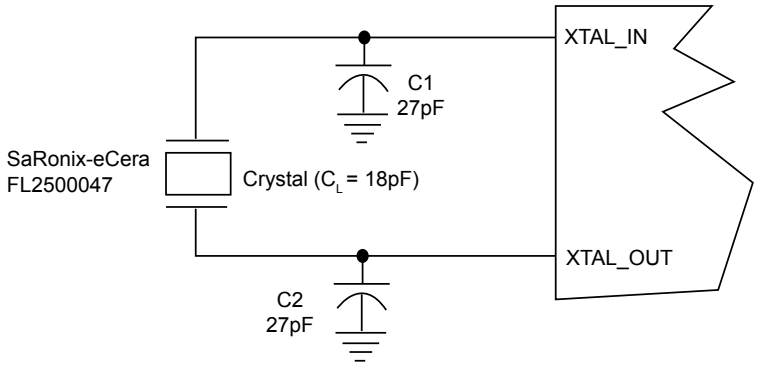
BYTE 7						
Bit	**Name**	**Control Function**	**Type**	**0**	**1**	**Default**
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

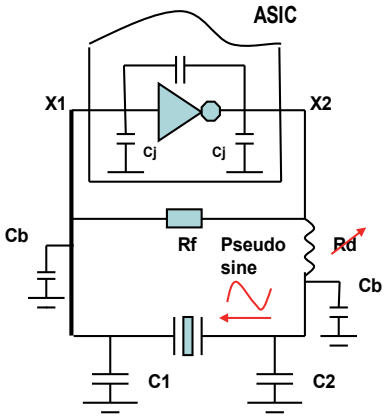
Application Notes

Crystal circuit connection

The following diagram shows crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit





CL= crystal spec. loading cap.

Cj = chip in/output cap. (3~5pF)

Cb = PCB trace/via cap. (2~4pF)

C1,2 = load cap. components

Rd = drive level res. (100Ω)

Final choose/trim C1=C2=2 *CL - (Cb +Cj) for the target +/-ppm
Example: C1=C2=2*(18pF) – (4pF+5pF)=27pF

Recommended Crystal Specification

Pericom recommends:

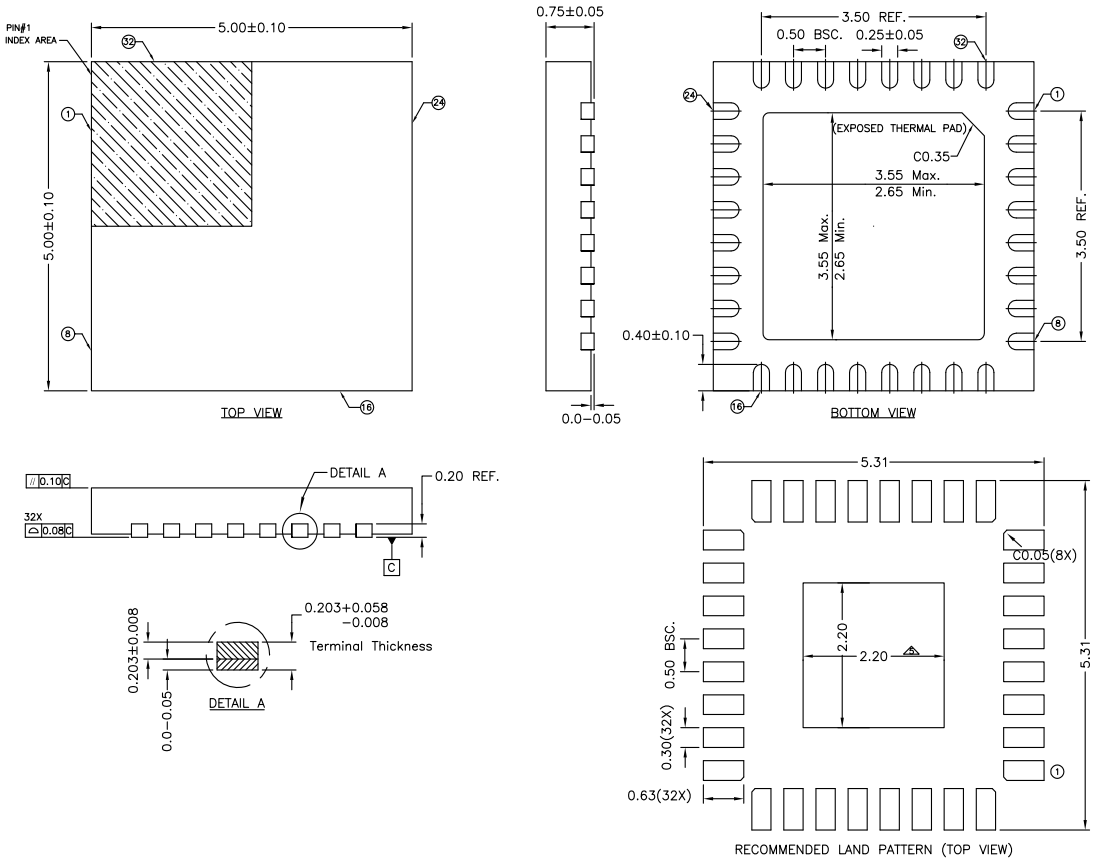
a) FL2500047, SMD 3.2X2.5(4P), 25MHz, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Thermal Characteristics

Symbol	Parameters	Condition	Min.	Type	Max.	Units
θJA	Thermal Resistance Junction to Ambient	Still air		44.7		°C/W
θJA	Thermal Resistance Junction to Case			21.7		°C/W

Packaging Mechanical: 32-Pin TQFN (ZH)



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencile design is recommended)

PERICOM Enabling Serial Connectivity — **DATE: 06/30/11**

DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH32

DOCUMENT CONTROL #: PD-2070 — **REVISION: B**

11-0147

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information[1-3]

Ordering Code	Package Code	Description
PI6CFGL401BZHIE	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)
PI6CFGL401BZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN), Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel