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Kind regards,

Team Nexperia

PSMN013-80YS

N-channel LPAK 80 V 12.9 m Ω standard level MOSFET

Rev. 01 — 25 June 2009

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

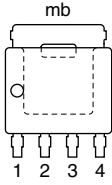
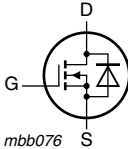
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	-	80	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	60	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	106	W
T _j	junction temperature		-55	-	175	°C
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 55 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω ; unclamped	-	-	70	mJ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 40 V; see Figure 14 ; see Figure 15	-	8	-	nC
Q _{G(tot)}	total gate charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 40 V; see Figure 14 ; see Figure 15	-	37	-	nC
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see Figure 12	-	-	19.8	m Ω
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see Figure 13	-	9.7	12.9	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

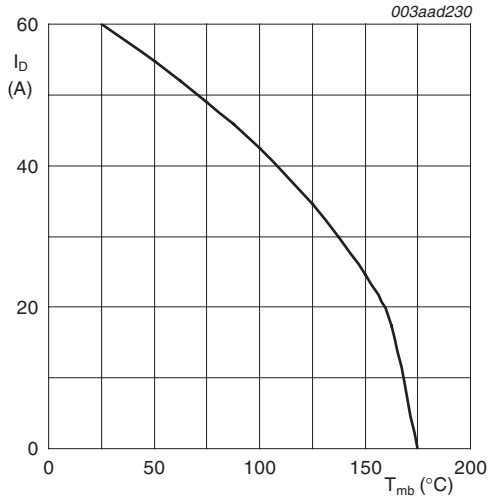
Type number	Package		Version
	Name	Description	
PSMN013-80YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

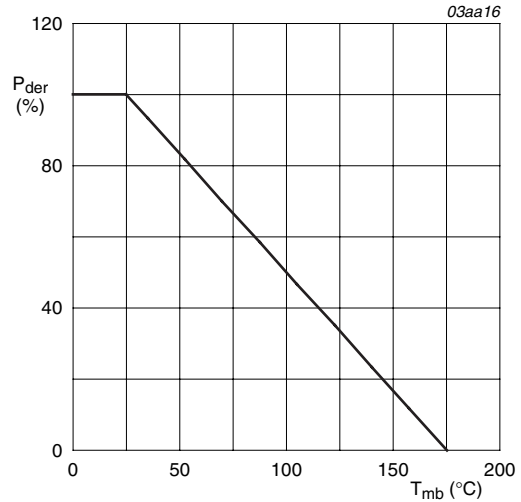
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	42	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	60	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	233	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	106	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	60	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	233	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 55\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	70	mJ



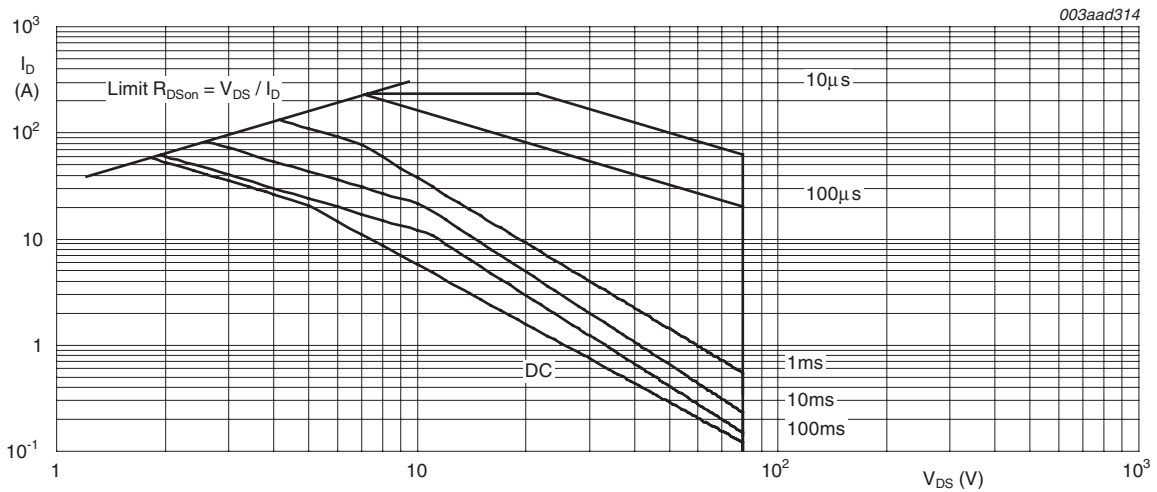
$V_{GS} \geq 10V$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	1.4	K/W

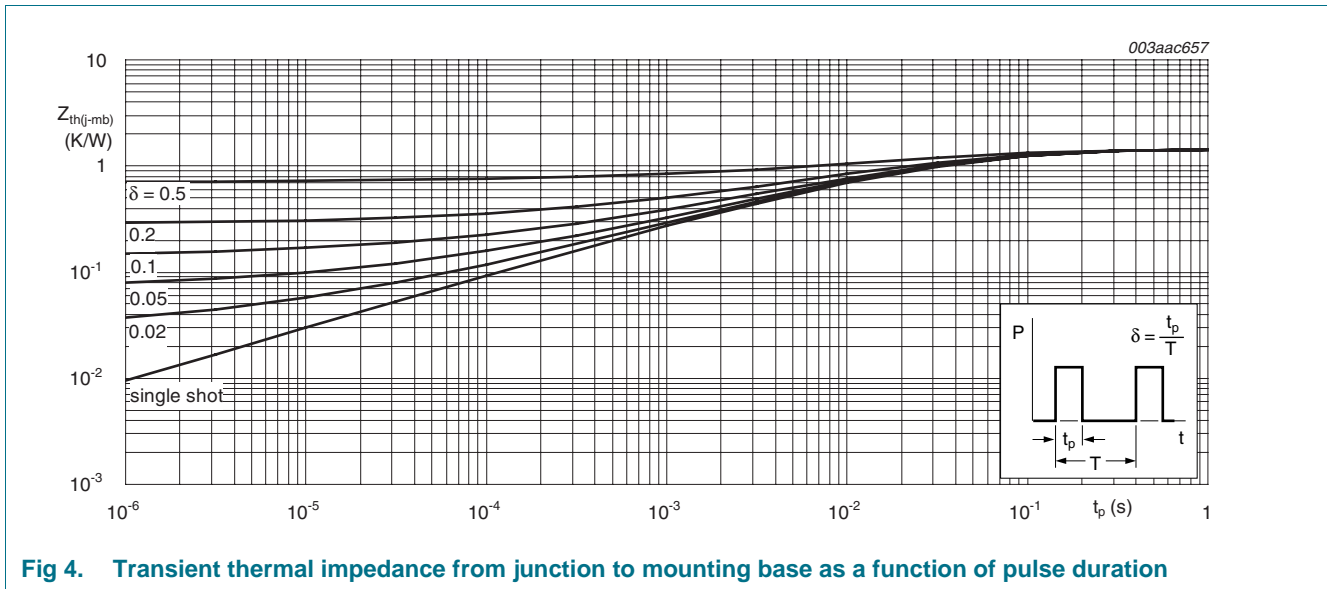


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	73	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10 ; see Figure 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10 ; see Figure 11	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 10 ; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	3	μA
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	40	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C$; see Figure 12	-	-	31	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C$; see Figure 12	-	-	19.8	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$; see Figure 13	-	9.7	12.9	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.68	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	31	-	nC
		$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	37	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	11	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 40 V$	-	4.8	-	V
C_{iss}	input capacitance	$V_{DS} = 40 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 16	-	2420	-	pF
C_{oss}	output capacitance		-	224	-	pF
C_{rss}	reverse transfer capacitance		-	125	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 V;$	-	20	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \text{ } \Omega$	-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
t_f	fall time		-	10	-	ns

Table 6. Characteristics ...continued
 Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.84	1.2	V
t_{rr}	reverse recovery time	$I_S = 50\text{ A}$; $di_S/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	52	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$	-	91	-	nC

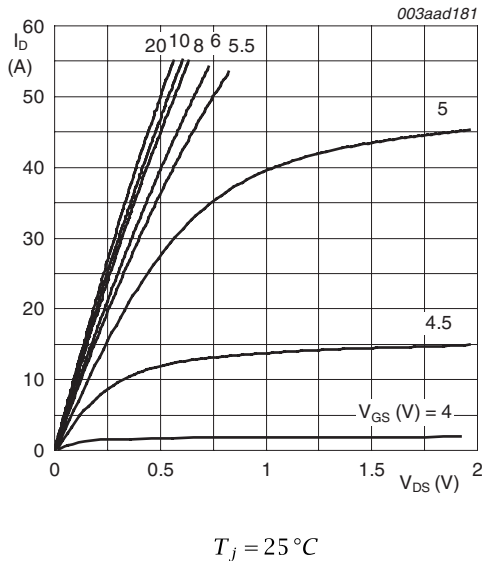


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

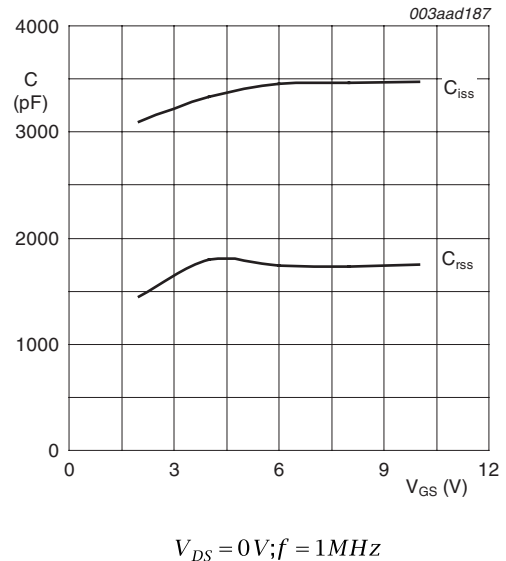


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

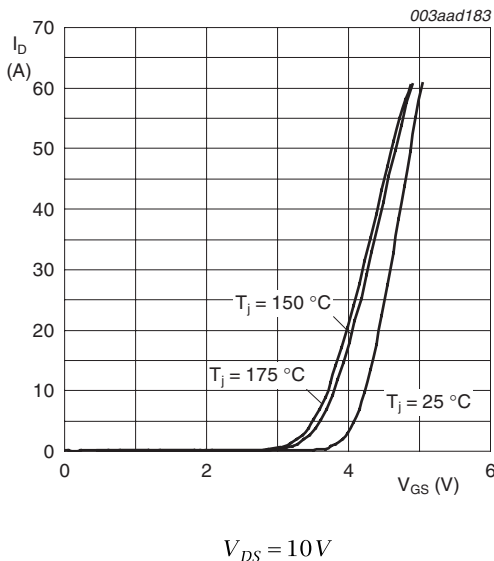


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

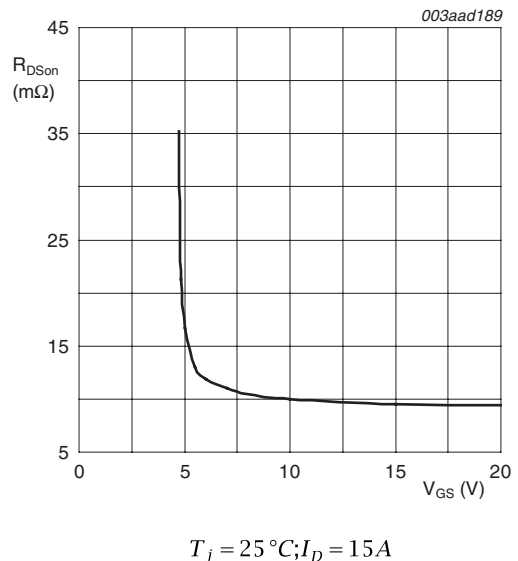
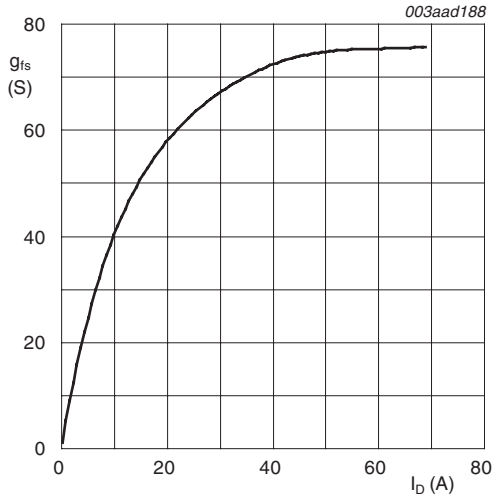
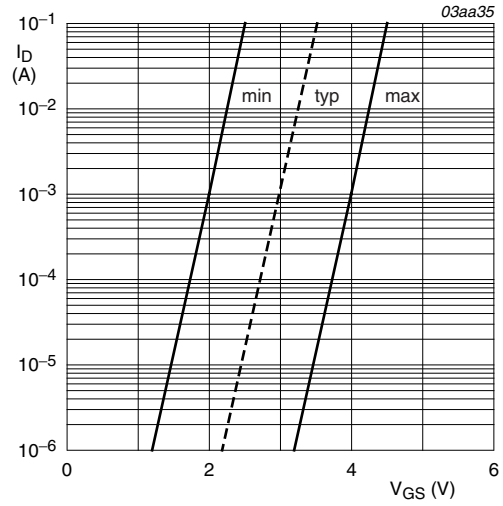


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



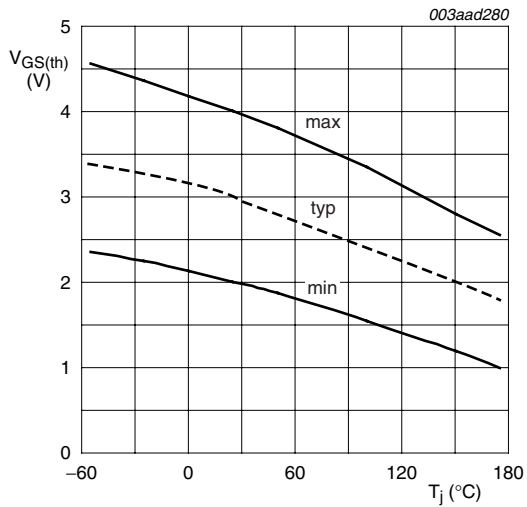
$$V_{DS} = 25 V$$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



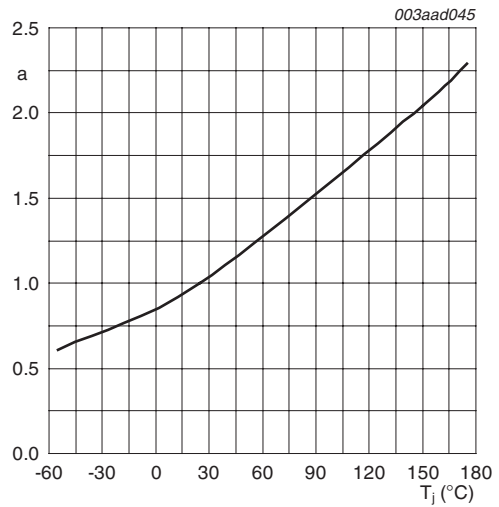
$$T_j = 25^\circ C; V_{DS} = 5 V$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



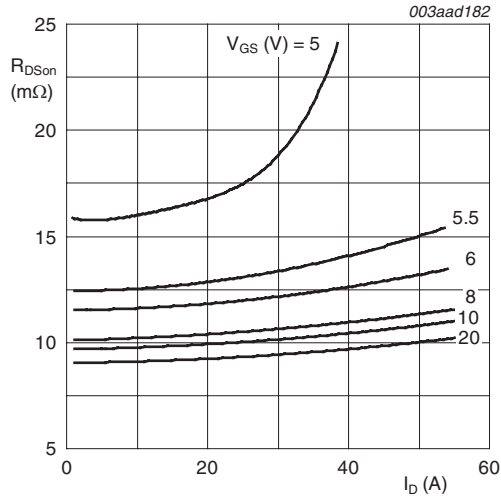
$$I_D = 1 mA; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

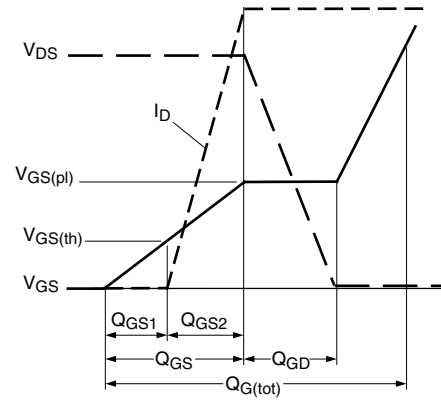
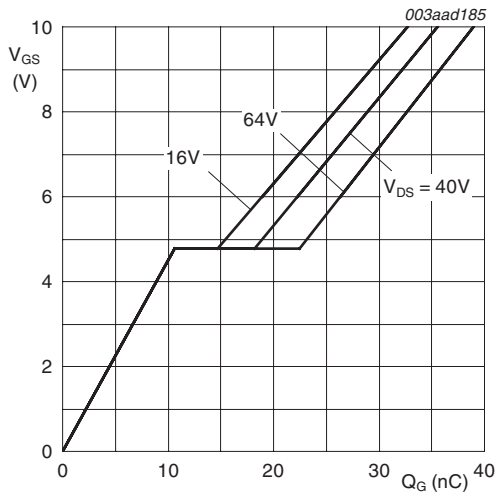
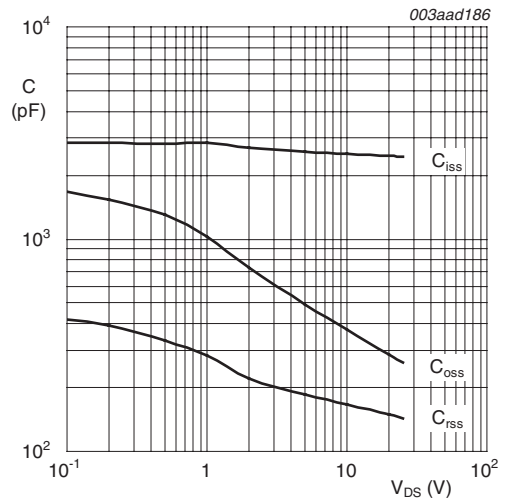


Fig 14. Gate charge waveform definitions



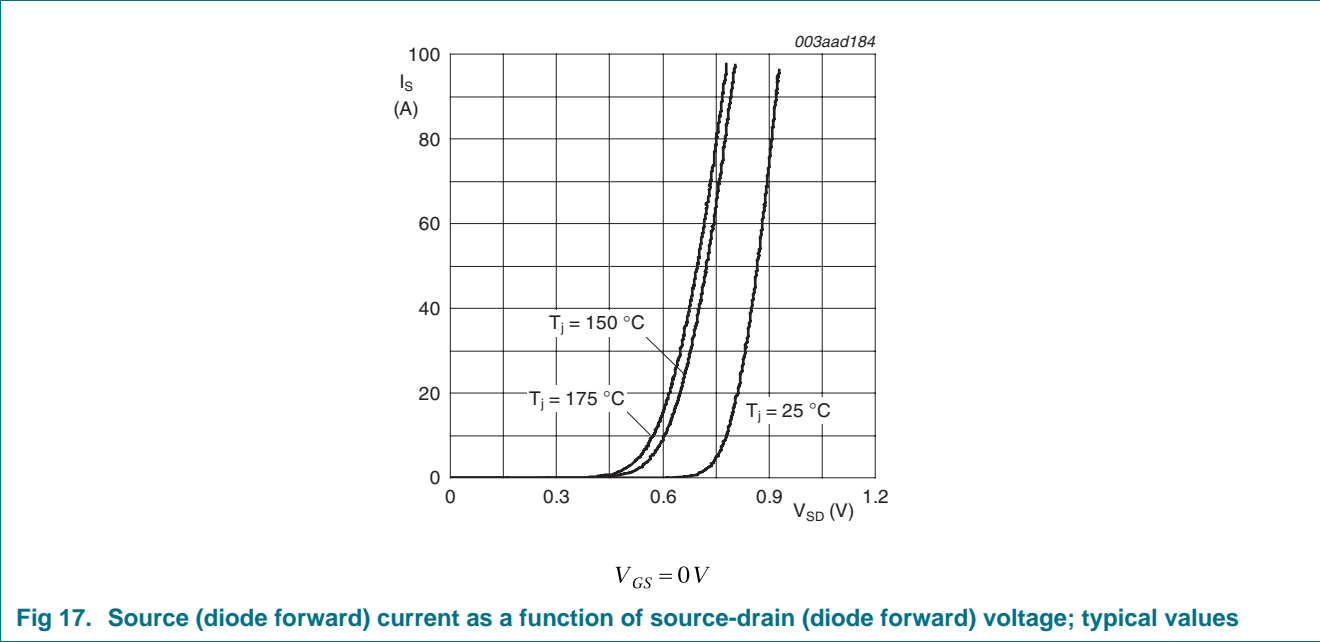
$T_j = 25^\circ C; I_D = 10 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

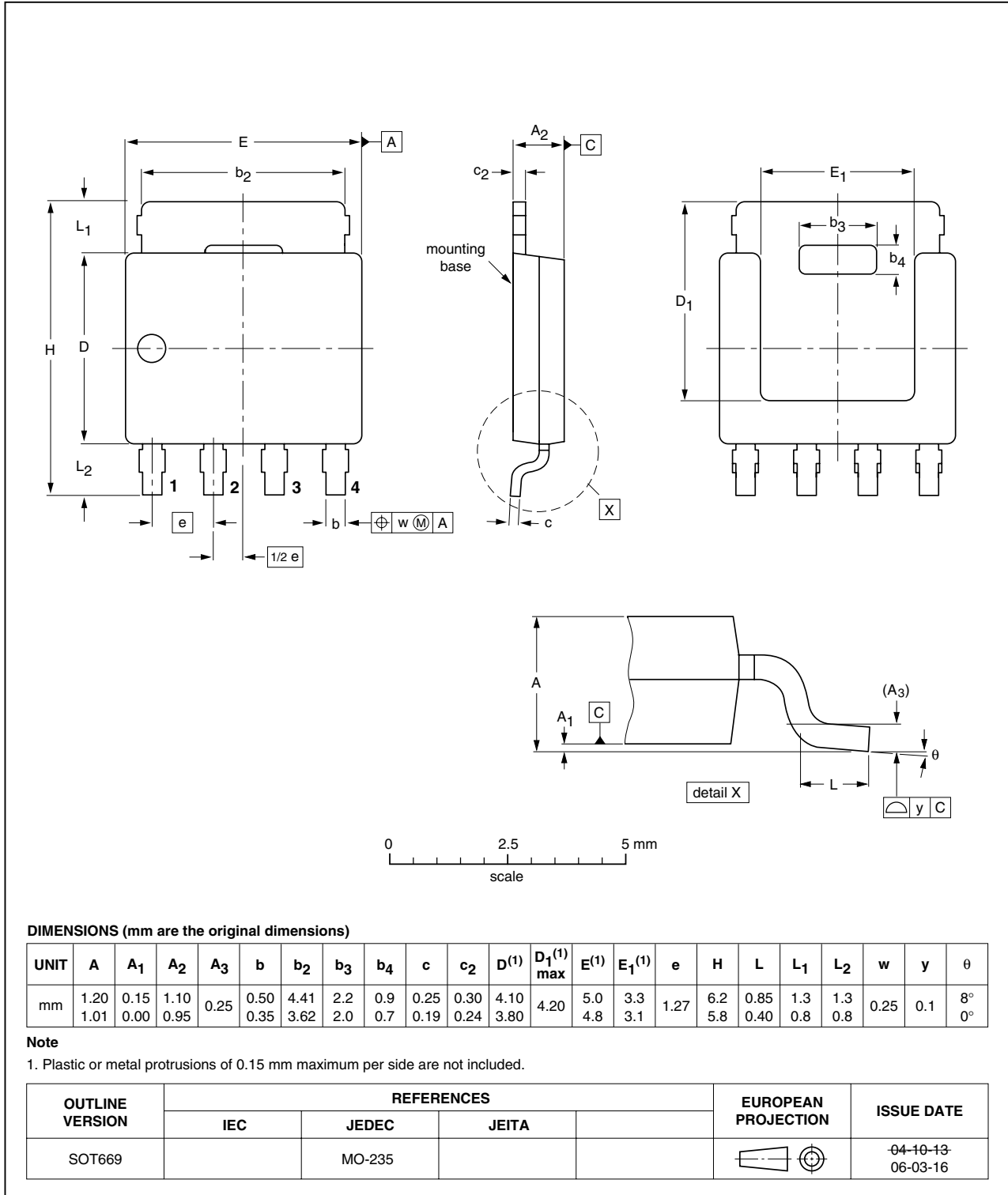


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN013-80YS_1	20090625	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	10
8	Revision history	11
9	Legal information	12
9.1	Data sheet status	12
9.2	Definitions	12
9.3	Disclaimers	12
9.4	Trademarks	12
10	Contact information	12

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