

NVMFD5C462N

Power MOSFET

40 V, 5.4 mΩ, 70 A, Dual N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C462NWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	40	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	70	A
		$T_C = 100^\circ\text{C}$	49	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	50	W
		$T_C = 100^\circ\text{C}$	25	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	17.6	A
		$T_A = 100^\circ\text{C}$	12.5	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	3.2	W
		$T_A = 100^\circ\text{C}$	1.6	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	298	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	41.7	A	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_{L(pk)} = 5 \text{ A}$)	E_{AS}	146	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	3	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

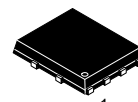
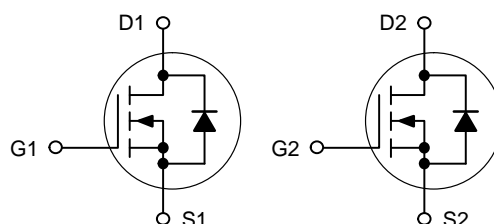


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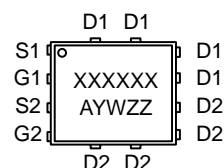
$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	5.4 mΩ @ 10 V	70 A

Dual N-Channel



DFN8 5x6 (SO8FL) CASE 506BT

MARKING DIAGRAM



XXXXXX = 5C462N (NVMFD5C462N)
or 462NWF (NVMFD5C462NWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			23		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C		10	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	2.5		3.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-6.5		mV/°C
Drain-to-Source On Resistance	R _{DSON}	V _{GS} = 10 V, I _D = 25 A		4.5	5.4	mΩ

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		1020		pF
Output Capacitance	C _{OSS}			550		
Reverse Transfer Capacitance	C _{RSS}			21		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V; I _D = 25 A		16		nC
Threshold Gate Charge	Q _{G(TH)}			3.0		
Gate-to-Source Charge	Q _{GS}			5.0		
Gate-to-Drain Charge	Q _{GD}			2.8		
Plateau Voltage	V _{GP}			4.8		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 25 A, R _G = 1.0 Ω		12		ns
Rise Time	t _r			30		
Turn-Off Delay Time	t _{d(OFF)}			26		
Fall Time	t _f			10		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 25 A	T _J = 25°C		0.86	1.2	V
			T _J = 125°C		0.75		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 25 A		29		ns	
Charge Time	t _a			14			
Discharge Time	t _b			14			
Reverse Recovery Charge	Q _{RR}			12			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

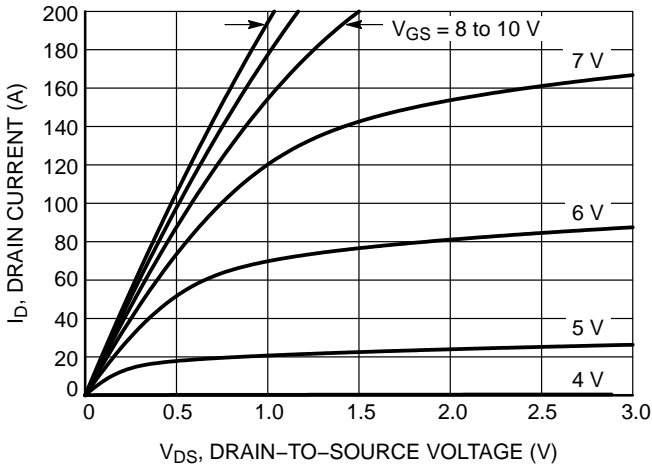


Figure 1. On-Region Characteristics

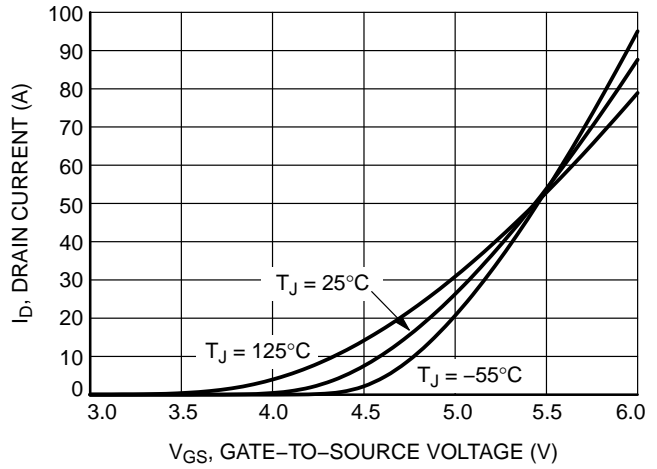


Figure 2. Transfer Characteristics

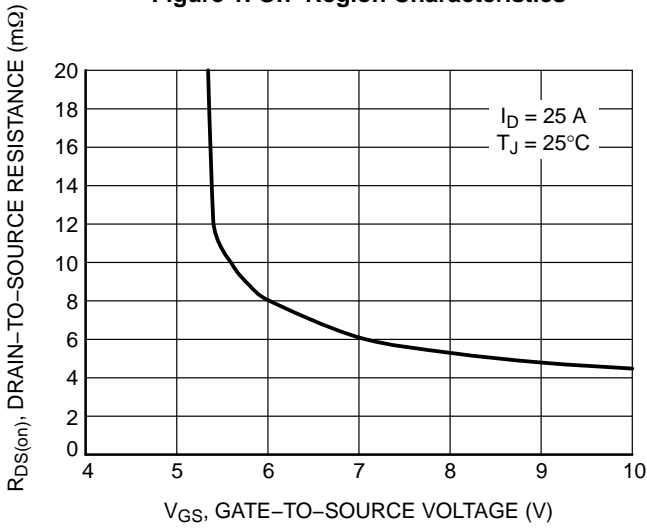


Figure 3. On-Resistance vs. Gate-to-Source Voltage

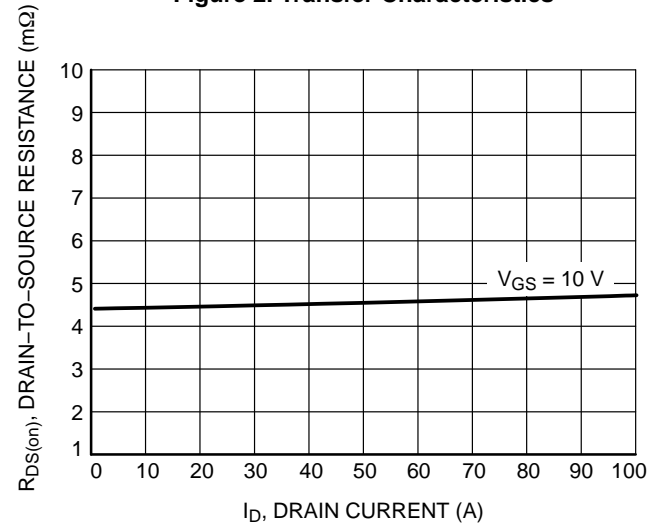


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

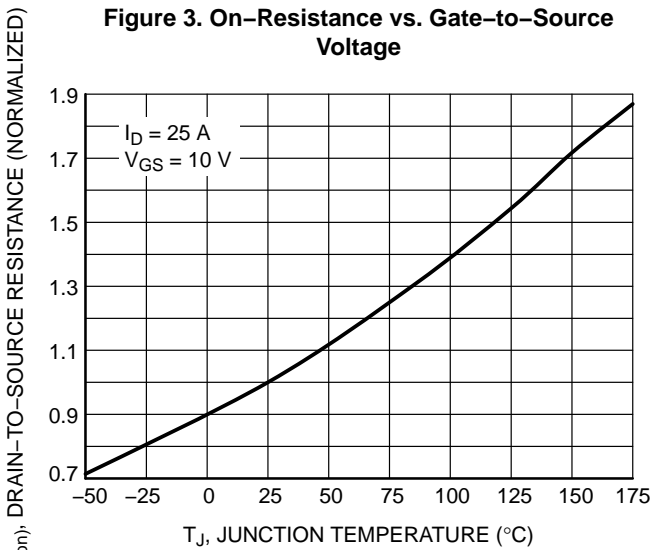


Figure 5. On-Resistance Variation with Temperature

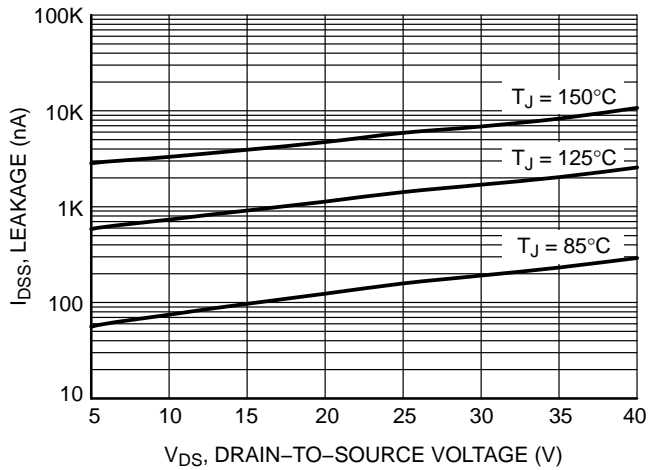


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

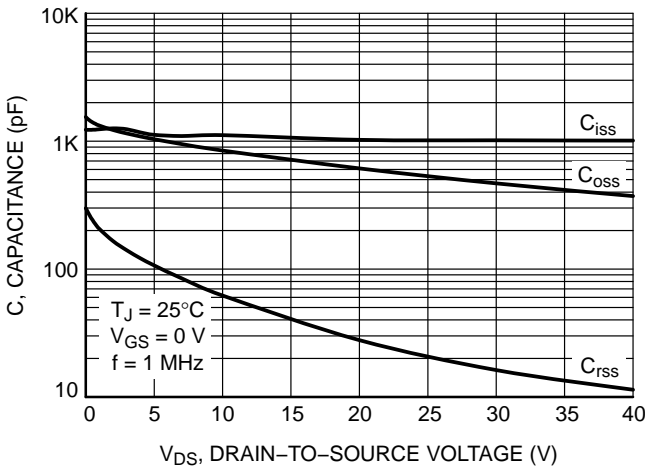


Figure 7. Capacitance Variation

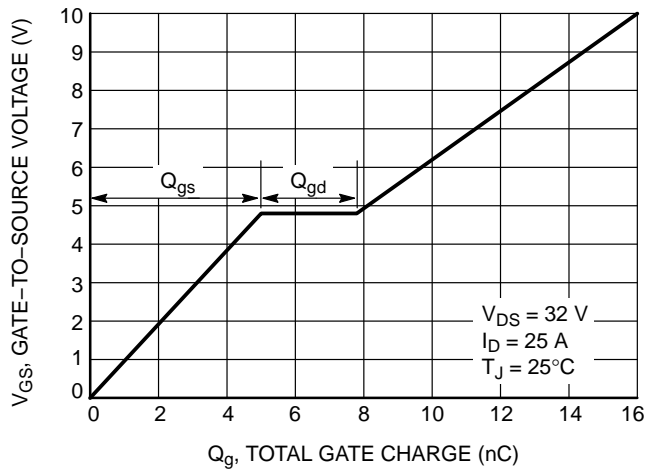


Figure 8. Gate-to-Source vs. Total Charge

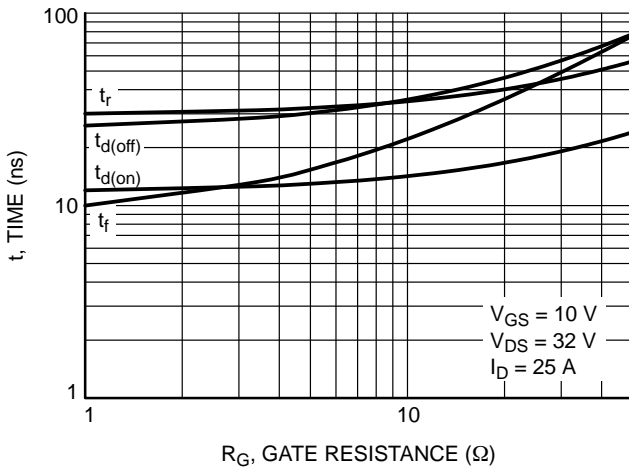


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

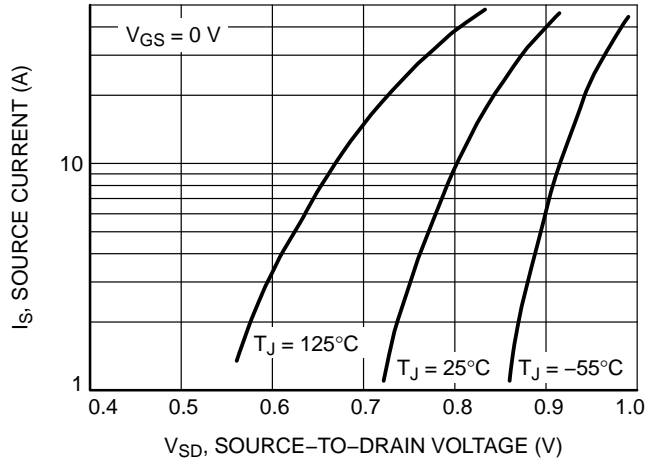


Figure 10. Diode Forward Voltage vs. Current

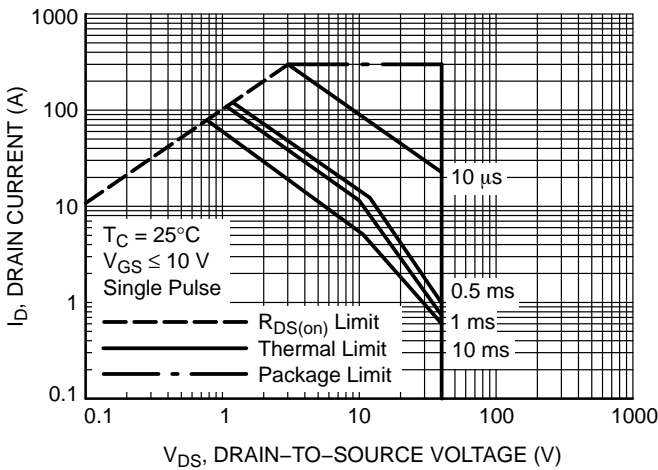


Figure 11. Maximum Rated Forward Biased Safe Operating Area

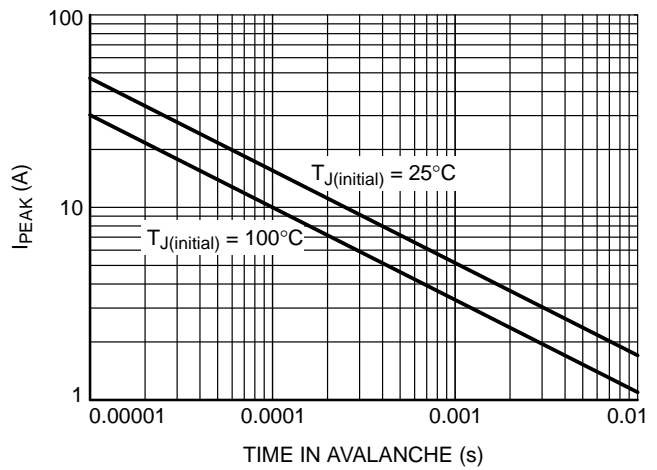


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

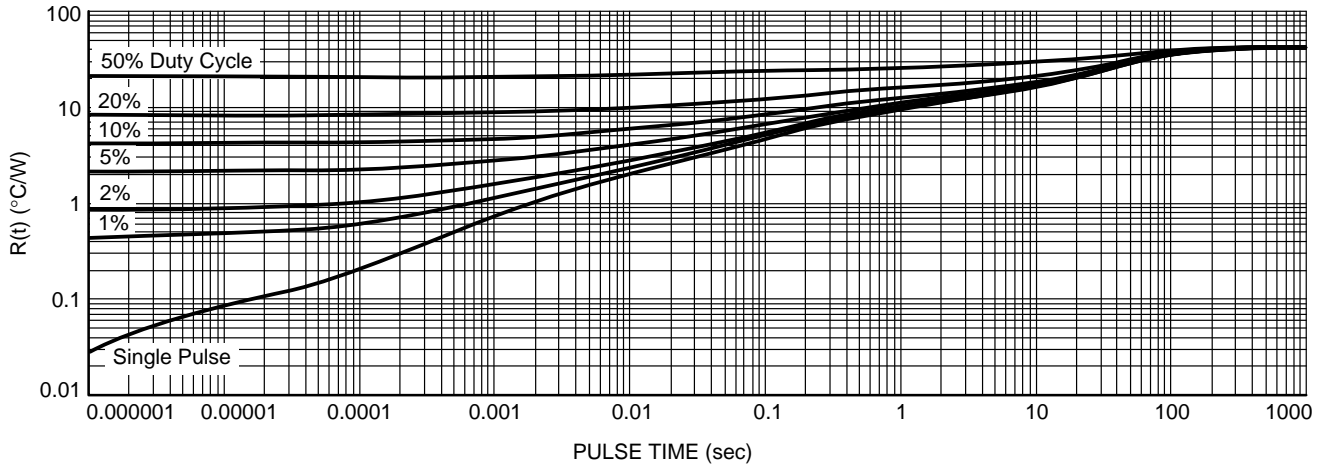


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFD5C462NT1G	5C462N	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5C462NWFT1G	462NWF	DFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

