Dual, High and Low Side ORing Application Using PICOR's PI2003 and PI2007

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Introduction

When designing redundant power systems, the ability to isolate a failed power source from the working power source is critical in maintaining uninterrupted operation of the load circuitry. To achieve this ability, the power sources are "OR'ed" together through fast-acting diodes (Figure 1), which will quickly isolate a shorted or disabled source from the OR'ed output supply by simply reverse biasing the diode. This method works very well and is relatively inexpensive to implement. The downside of using diodes is that the inherent voltage drop they have will reduce overall power efficiency when used at higher currents.

To significantly improve efficiency and still retain the isolation protection of the ORing diodes, a MOSFET can be used, in conjunction with a controller, to replace the ORing diodes (Figure 2). When current flows from the input source to the output redundant bus, the controller senses the direction of the current flow and will turn the MOSFET "on" and drive it into its minimum on-state resistance ($R_{DS(on)}$) value. The power dissipated in the MOSFET is the value of the current squared, multiplied by the MOSFET's $R_{DS(on)}$ resistance. Since this resistance is very low, the power loss is much less than the loss across a diode. When the controller senses a reversal of current flow from the OR'ed output supply back to the input power source, the controller responds quickly to turn-off the MOSFET and the MOSFET's parasitic body diode will then isolate the OR'ed output redundant bus from the failed input supply.

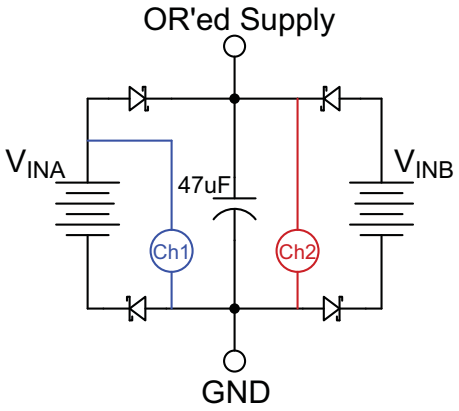


Figure 1 – *Diode OR'ed Supplies*

The Active ORing circuit in Figure 2 uses both the PI2003, to control the low-side MOSFET, and the PI2007, to control the high-side MOSFET. Since Active ORing components are not designed to enhance current sharing between the supplies, one of the supplies will dominate and provide the current to the load. The PI2003 has a low-current fault feature that is used to either enable or disable the PI2007 associated with it. If there is little or no current through the PI2003 it issues a fault condition that pulls its $\overline{FT}$ pin low. The MOSFET that is used to provide a return path for the PI2007 bias supply is then disabled, which in turn disables the PI2007. If the input supply is still in-circuit, then the PI2003 will remain powered up and will continue to monitor the supply. If the supply were to be removed or disabled, then the supply to the PI2003 would be discharged and the PI2003 would disable its MOSFET. The resulting circuit would be just the two parasitic body diodes of the high and low side MOSFETs.

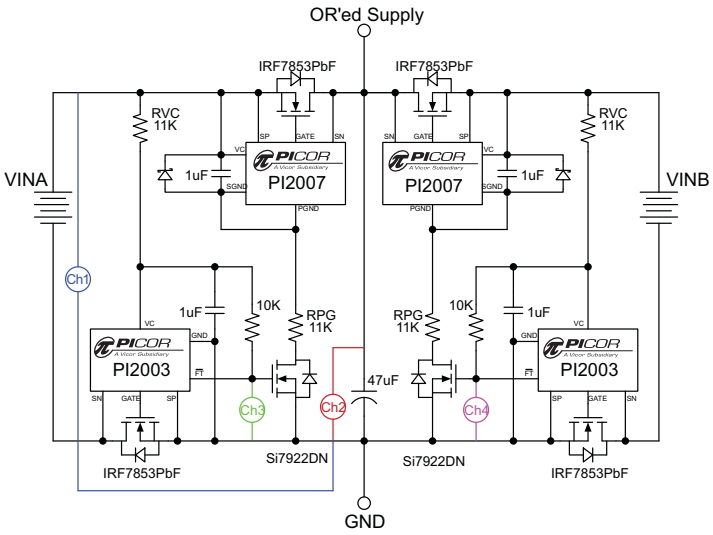


Figure 2 – *PI2003 / PI2007 FET OR'ed supplies*

PI2003 / PI2007 ORing Performance

The waveforms in Figure 3 represent the performance of the diode ORing circuit shown in Figure 1. Channel 1 (blue) is the voltage seen on the input supply "A" rail; channel 2 (red) is the OR'ed output voltage. Both waveforms are referenced to the OR'ed output GND and are DC measurements with a 30 V offset.

Prior to shorting the "VINA" supply at 200 us, the voltage measured on "VINA" is approximately a diode higher than the OR'ed output voltage. The voltage of "VINB" is purposely set to be 700 mV lower that "VINA" so that "VINA" is the dominate supply.

Once the short occurs, the voltage on "VINA" drops off the screen and the OR'ed output voltage will start to decay to the value of "VINB", minus the diode drop. When compared to the original value of "VINA", this difference is about 1.6 V. The drop in the OR'ed output voltage is the difference in the set voltage of the two input supplies, about 700 mV.

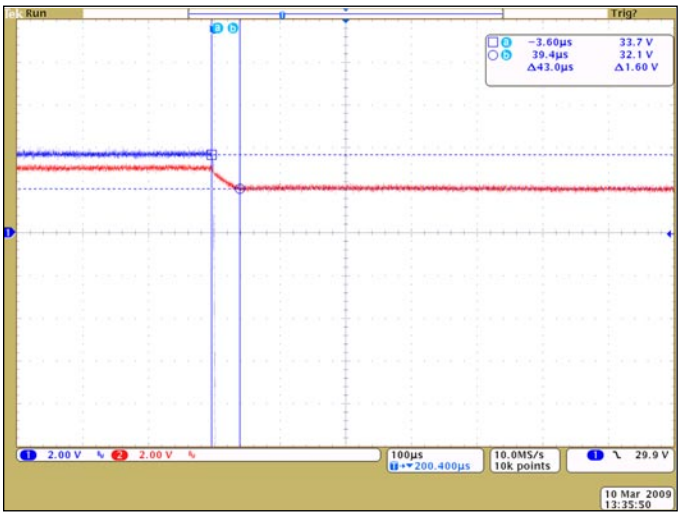


Figure 3 – *Diode ORing*

The waveforms in Figure 4 represent the active ORing circuit shown in Figure 2. Prior to the short, the OR'ed output voltage and the voltage of "VINA" are the same due to the very low impedance of the MOSFET in its "on" state. Once the "VINA" supply (blue) is shorted, the OR'ed output voltage (red) begins to drop to the value of "VINB", minus the ORing FET's body-diode voltage drop. The $\overline{FT}$ pin of the PI2003 (pink) associated with the "VINB" supply begins to turn "on" once the OR'ed output voltage has decayed to the level where the load current in not being supplied by the OR'ed output capacitor. Once the $\overline{FT}$ pin is fully "on" it enables the PI2007 high-side ORing controller and less than 2 ms later the OR'ed output voltage is seen rising due to the high-side MOSFET being turned "on". Now the OR'ed output voltage is equal to the "VINB" voltage, which is still set to be ~700 mV lower than "VINA". The $\overline{FT}$ pin of the PI2003 associated with the "VINA" supply (green) shuts off shortly after the short-circuit event due to the fact that the PI2007 was first to react to the short circuit and has shut itself "off", isolating the short from the OR'ed output supply. With no voltage source available to power the PI2003, the PI2003 shuts off its MOSFET once its supply (VC) pin passes below the under-voltage fault level.

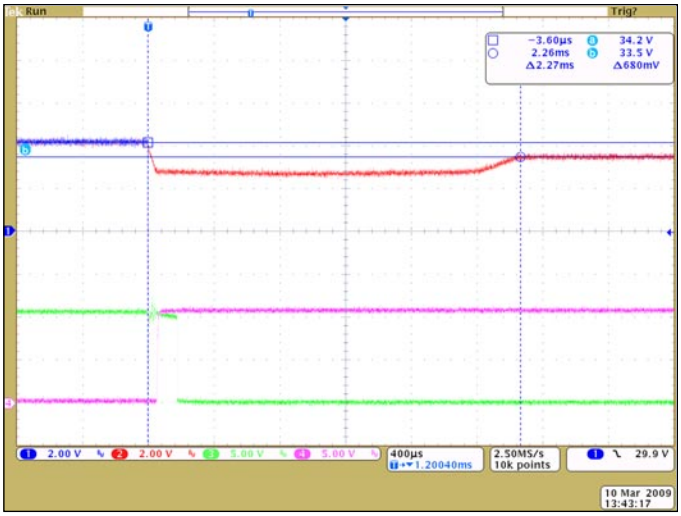


Figure 4 – *Active ORing, Using MOSFET's*

Design/Safety Concerns

In the event that a power feed is not shorted, but is instead disabled or removed, the response of the FET ORing circuit must be to completely isolate the input terminals to the OR'ed output supply. If the circuit in Figure 2 were designed without the MOSFET's that enable the high side PI2007 controller (Figure 5), there can be conditions where the OR'ed output voltage can appear on the input terminals even without a supply being connected. This condition could pose a potential safety hazard.

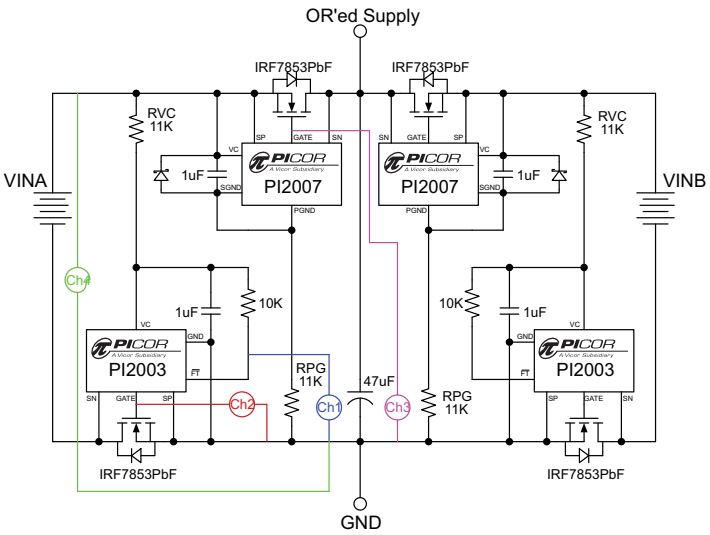


Figure 5 – *Active ORing circuit with PI2003 and PI2007 enabled by OR'ed output.*

With the high- and low-side MOSFETs in Figure 5 fully "on" for either input supply, the removal of that supply creates a high-impedance path made up of the 11 k RPG resistor and the voltage drop across the PI2007. The reversed current in this path is not enough to trigger a "reverse current fault condition", where the controllers would turn "off" their respective MOSFETs. Effectively, the OR'ed output voltage is present on the supply input nodes without the supply being connected, as shown in Figure 6.

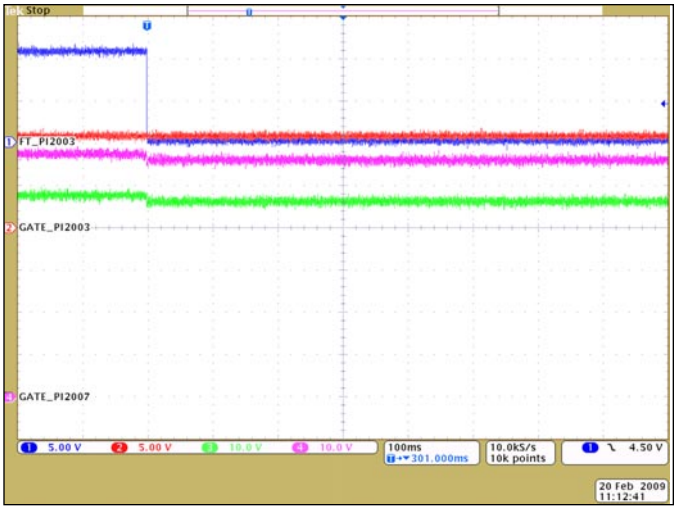


Figure 6 – *VINA Supply unplugged, ORing MOSFETs remained in RDS(on) minimum state.*

The circuit in Figure 7 illustrates the use of the $\overline{FT}$ signal of the PI2003 to disable the PI2007; by opening the power return path from ground and forcing the high-side ORing MOSFET to shut off. With the high-side MOSFET "off", the positive path of the OR'ed output voltage is isolated from the positive input voltage node. With no positive input voltage present, and no connection to the OR'ed output voltage supply, the low-side controller's supply (VC) decays until it reaches the under-voltage fault level of the PI2003 and shuts off the MOSFET. With both the high and low side MOSFET "off', the inputs are completely isolated from the OR'ed output supply.

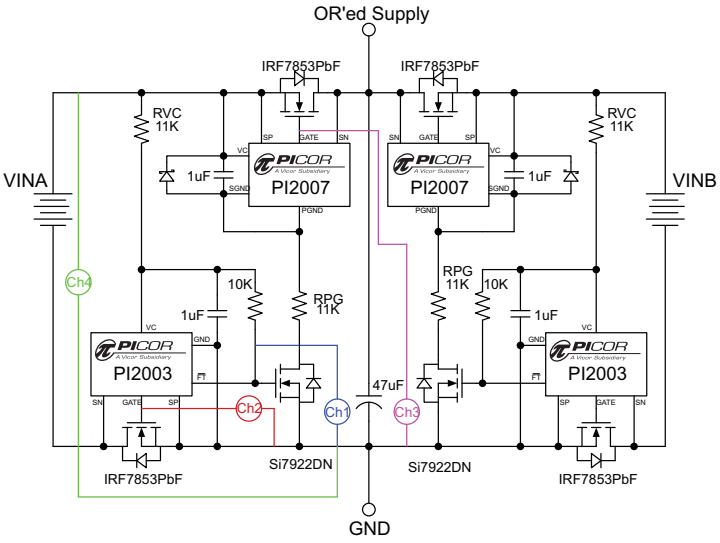


Figure 7 – *Active ORing circuit with PI2003 and PI2007 enabled by OR'ed output.*

The waveforms in Figure 8 show the response of the circuit in Figure 7 to an input supply being disabled, but still in-circuit. When the input supply is disabled, the current to the OR'ed output load is now provided by the alternate input supply, making the PI2003 of the "disabled" supply issue a low-current fault on its $\overline{FT}$ pin (blue). Pulling the $\overline{FT}$ pin low shuts off the MOSFET that provides the power return path of the PI2007. With its power return path "open", the PI2007's supply (VC) rail starts to decay and will turn off its MOSFET drive once an under-voltage fault level is reached (pink). The high-side MOSFET gate drive is charged-pumped by the PI2007 to be about 10 V higher than VIN. The gate voltage can be seen to go from about 10 V greater than VIN to about 10 V lower, which is the voltage seen on the PI2007's power return pin. As the voltage across the PI2007's VC bypass capacitor decays, the difference in voltage between the high-side gate and VIN decays as well until they are equal. As VIN continues to decay the supply to the PI2003 also decays until it too reaches an under-voltage fault level and turns off its MOSFET (red).

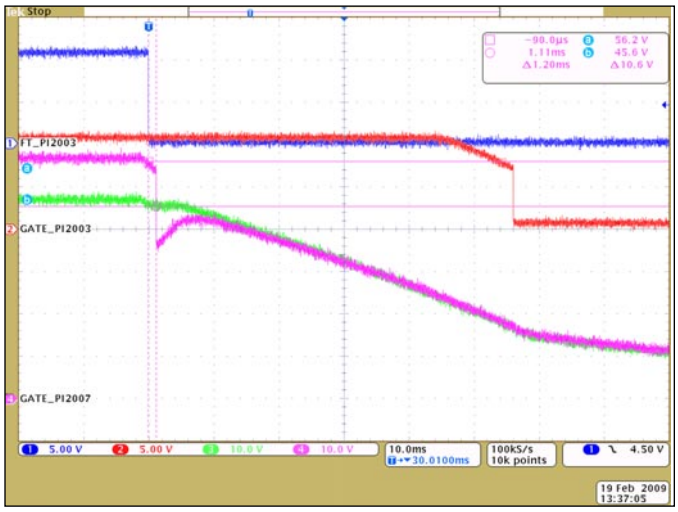


Figure 8 – *VINA Supply disabled, but left in-circuit.*

In Figure 9, the supply was completely removed from the circuit with essentially the same results as the disabled supply. The time for the VIN discharge was greater with the removed supply since the impedance of the "disabled" versus the "opened" supply is much lower and will discharge the input quicker. The addition of some "bleeder" resistors can decrease this time to more closely resemble the "disabled" supply waveforms.

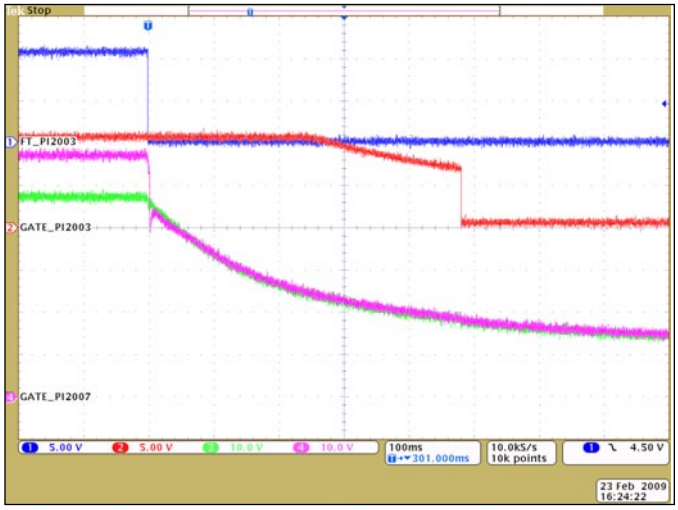


Figure 9 – *VINA Supply removed from circuit.*

Active ORing Timing Diagrams

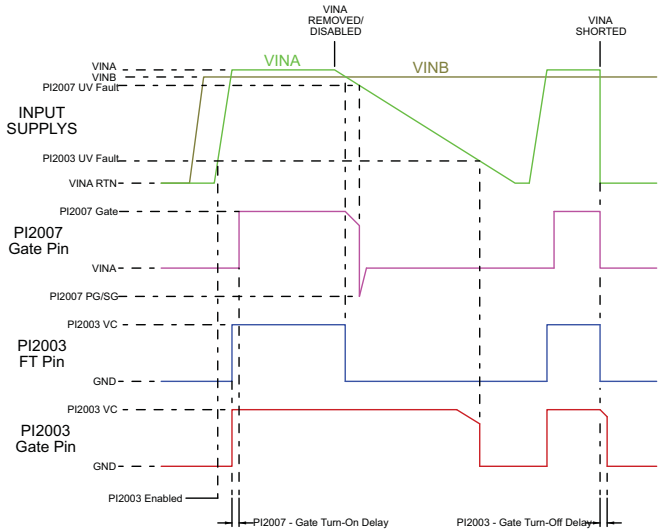


Figure 10 – *Typical Timing Waveforms of the PI2007 and PI2003.*

In Figure 10, the V_{INB} supply is shown reaching its peak value first to illustrate that the PI2003 and PI2007 that are associated with the V_{INA} supply are not active until the V_{INA} supply starts to ramp up. Once the V_{INA} supply surpasses the value of the V_{INB} supply, the system current will be provided by the V_{INA} supply and the PI2003 will release its $\overline{FT}$ pin (blue) to enable the supply of the PI2007 and will turn "on" its ORing MOSFET (red). A short time later, the PI2007 will turn "on" the gate of the high side MOSFET (pink) and both ORing MOSFETs will be at their RDS(on) minimum value. The gate voltage of the PI2007 (pink) is about 10 V higher than V_{INA} and typically turns on in under 1 ms.

When the V_{INA} supply is disabled or removed from the system, the PI2003 senses the loss of current flow (light load current fault) and will disable the supply of the PI2007 by asserting its $\overline{FT}$ pin "low". The gate pin of the PI2007 will keep the high-side MOSFET "on" and maintain a gate voltage greater than the VINA voltage until the voltage across its bypass capacitor, connected between the PI2007's VC and PG/SG pins, decays to the point where it causes an under-voltage fault within the PI2007. The PI2007 will then turn "off" its gate drive, which drops to the value of PG/SG. As the bypass capacitor decays the gate voltage eventually follows the value of V_{INA}. After the PI2007 has shut off and as the V_{INA} voltage continues to decay, the PI2003's gate voltage will start to drop due to the decaying of the voltage across its bypass capacitor. Once the voltage has passed below the under-voltage fault level of the PI2003 the gate of the low-side MOSFET is turned "off" and now both ORing MOSFETs are disabled, leaving their parasitic body diodes to provide the electrical isolation between the OR'ed output voltage and the input leads.

Reestablishment of the V_{INA} supply re-enables the PI2003 and PI2007 ORing devices and their associated MOSFETs. If a short occurs across the inputs of the V_{INA} supply, the PI2007 responds first and disables its MOSFET, isolating the V_{INA} supply from the OR'ed output voltage. With the loss of the V_{INA} supply, the PI2003 eventually losses its supply voltage and turns off its MOSFET.

Preventing leakage current from one input supply to another is a feature of ORing diodes that also needs to be replicated when using ORing MOSFET's. The ability of the PI2003 to disable the PI2007's high-side ORing MOSFET makes this possible.

Once the input voltage is greater than the UVLO of the PI2003 it will turn on its MOSFET shorting the input voltage return to the OR'ed output voltage return. With both input supplies, V_{INA} and V_{INB}, at this voltage level or greater, both PI2003s will turn on their MOSFETs. This will effectively short the returns of V_{INA}, V_{INB} and the OR'ed supply together. Whichever supply is the first to supply the load current will enable its PI2007 and associated high side MOSFET. The supply not sourcing the load current will have a low current fault that will keep its PI2007 controller and high-side MOSFET disabled.

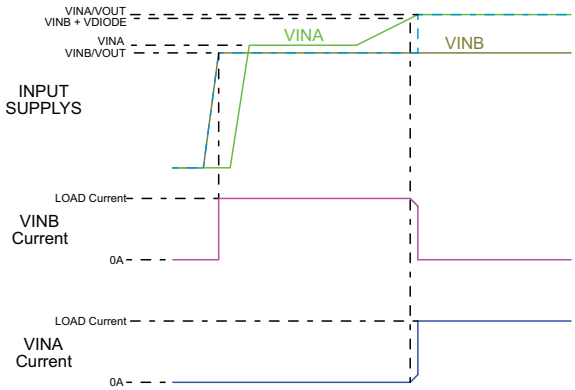


Figure 11 – *Load current transitioning between two input supplies.*

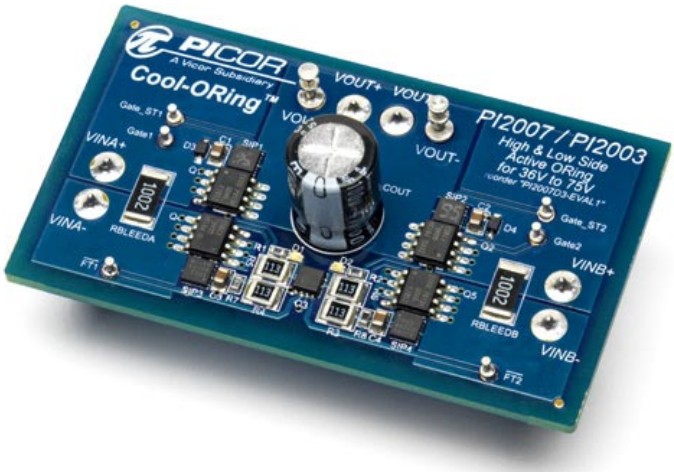
The powering up sequence of the supplies is not critical; they can be started together or one after the other. Their voltages are not critical; they can be the same or vastly different. If the voltages are the same, then one OR'ed side will turn on first and the other will stay off due to differing circuit parasitics, even when powered from the same supply. If the voltages are different, then the higher voltage will dominate, except when the voltage difference is less than the body diode voltage drop of the disabled ORing MOSFET. For example, if V_{INA} were 48 V and was applied to the circuit first, V_{INB} being 48.4 V and applied afterwards would not dominate and shut off the ORing circuit of V_{INA}. $V_{INB's}$ ORing circuit would remain disabled. For V_{INB} to dominate, its voltage would have to be increased to a level where it is greater than the body diode voltage of $V_{INB's}$ high side MOSFET. Once this voltage is exceeded, the V_{INB} supply will start to supply some portion of the load current to the OR'ed supply through the MOSFET's body diode. As $V_{INB's}$ voltage is increased, so will the amount of current it sources to the load. Once it reaches a point where the current it is sourcing is enough to clear the low current fault, the high-side MOSFET of V_{INB} will turn on and V_{INB} will now provide the total load current. Since $V_{INB's}$ voltage is now greater than $V_{INA's}$, the OR'ed output voltage will follow V_{INB} and V_{INA} will go into a low current fault and its high side MOSFET will be disabled.

The waveforms in Figure 11 depict the transitioning of the load current when the starting dominate supply (V_{INB}) is surpassed in voltage by an alternate supply (V_{INA}) and is disabled.

V_{INB} is the first supply sequenced and supplies the load current and determines the value of the OR'ed output voltage (V_{OUT}). Shortly after, the second supply (V_{INA}) is powered up, but it is not of a sufficiently greater voltage to assume the dominate position and provide the load current to V_{OUT}. As the voltage of V_{INA} is increased it eventually reaches a point where the body diode of V_{INA}'s high-side FET starts to conduct and delivers a small portion of the load current. The increasing V_{INA} voltage and current reaches the level where the low current fault of V_{INA}'s PI2003 is cleared and V_{INA}'s PI2007 is enabled, turning on the high-side MOSFET. With V_{INA}'s MOSFET "on", the output supply (V_{OUT}) now follows V_{INA} and it sources all of the current to the load. V_{INB}, being at a lower voltage potential and no longer being the source of the load current, gets disabled due to a low current fault. The only current that the non-dominate ORing supplies source is the current to power the PI2003.

Final Design Conclusion

By using the PI2003 controller's built-in "low-current-fault" monitor to enable or disable its paired PI2007 controller, the same system protection that is provided by ORing diodes can be achieved under any fault condition; while the lower power disipation of the MOSFET approach will provide a substantial power savings.



Picor PI2007D3-EVAL1, Dual High-side/ Low-side Evaluation Board

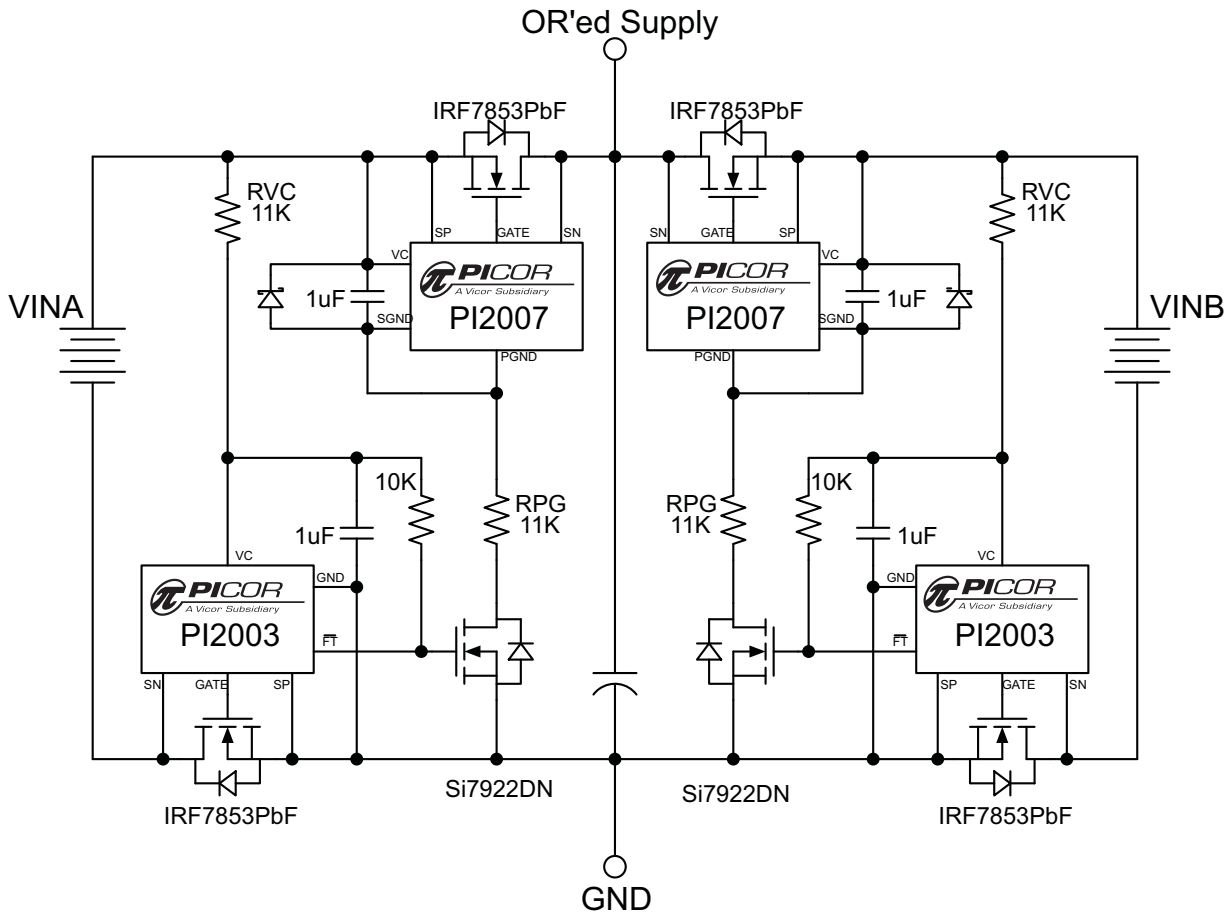


Figure 12 — *PI2003 biased to V_{IN}, used to enable/disable the PI2007.*