# LTC2201

## 16-Bit, 20Msps ADC

# FEATURES

- **Sample Rate: 20Msps**
- **81.6dB SNR and 100dB SFDR (2.5V Range)**
- **90dB SFDR at 70MHz (1.667V$_{P-P}$ Input Range)**
- **PGA Front End (2.5V$_{P-P}$ or 1.667V$_{P-P}$ Input Range)**
- **380MHz Full Power Bandwidth S/H**
- **Optional Internal Dither**
- **Optional Data Output Randomizer**
- Single 3.3V Supply
- Power Dissipation: 211mW
- Clock Duty Cycle Stabilizer
- Out-of-Range Indicator
- Pin Compatible Family
    - 25Msps: LTC2203 (16-Bit)
    - 10Msps: LTC2202 (16-Bit)
- 48-Pin (7mm × 7mm) QFN Package

# APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

# DESCRIPTION

The LTC®2201 is a 20Msps, sampling 16-bit A/D converter designed for digitizing high frequency, wide dynamic range signals with input frequencies up to 380MHz. The input range of the ADC can be optimized with the PGA front end.

The LTC2201 is perfect for demanding applications, with AC performance that includes 81.6dB SNR and 100dB spurious free dynamic range (SFDR). Maximum DC specs include ±5LSB INL, ±1LSB DNL (no missing codes).

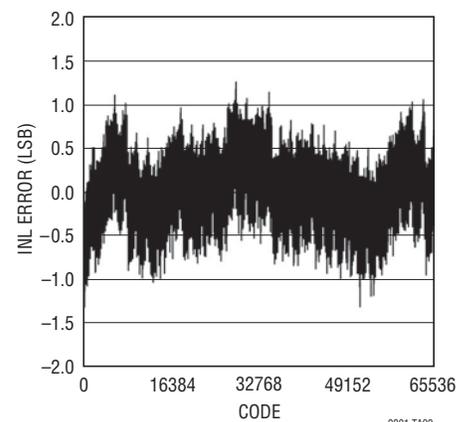A separate output power supply allows the CMOS output swing to range from 0.5V to 3.6V.

A single-ended CLK input controls converter operation. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

# TYPICAL APPLICATION
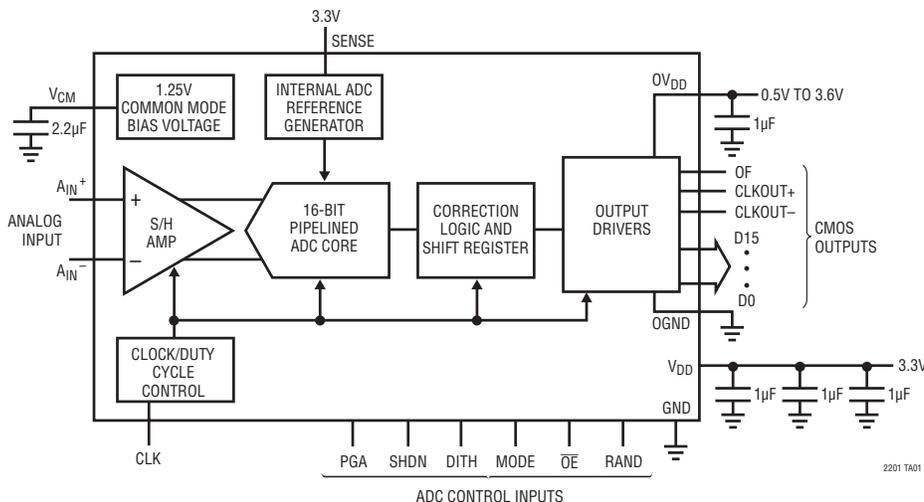


**Integral Nonlinearity (INL) vs Output Code**

# ABSOLUTE MAXIMUM RATINGS

**$OV_{DD} = V_{DD}$ (Notes 1 and 2)**

Supply Voltage ($V_{DD}$) .................................. −0.3V to 4V
Digital Output Supply Voltage ($OV_{DD}$) ......... −0.3V to 4V
Digital Output Ground Voltage (OGND) ........ −0.3V to 1V
Analog Input Voltage (Note 3) ..... −0.3V to ($V_{DD}$ + 0.3V)
Digital Input Voltage ................... −0.3V to ($V_{DD}$ + 0.3V)
Digital Output Voltage .............. −0.3V to ($OV_{DD}$ + 0.3V)
Power Dissipation ............................................ 2000mW
Operating Temperature Range
    LTC2201C ............................................... 0°C to 70°C
    LTC2201I ........................................... −40°C to 85°C
Storage Temperature Range ................. −65°C to 150°C

# PIN CONFIGURATION

TOP VIEW

Top pins (left to right): 48 GND, 47 PGA, 46 RAND, 45 MODE, 44 $\overline{OE}$, 43 OF, 42 D15, 41 D14, 40 D13, 39 D12, 38 OGND, 37 $OV_{DD}$

Left pins (top to bottom):
SENSE 1
$V_{CM}$ 2
$V_{DD}$ 3
$V_{DD}$ 4
GND 5
$A_{IN}^+$ 6
$A_{IN}^-$ 7
GND 8
GND 9
CLK 10
GND 11
$V_{DD}$ 12

Center: 49

Right pins (top to bottom):
36 $OV_{DD}$
35 D11
34 D10
33 D9
32 D8
31 OGND
30 CLKOUT$^+$
29 CLKOUT$^-$
28 D7
27 D6
26 D5
25 $OV_{DD}$

Bottom pins (left to right): $V_{DD}$ 13, $V_{DD}$ 14, GND 15, SHDN 16, DITH 17, D0 18, D1 19, D2 20, D3 21, D4 22, OGND 23, $OV_{DD}$ 24

UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

EXPOSED PAD IS GND (PIN 49)
MUST BE SOLDERED TO PCB BOARD
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 29°C/W

# ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2201CUK#PBF | LTC2201CUK#TRPBF | LTC2201UK | 48-Lead (7mm × 7mm) Plastic QFN | 0°C to 70°C |
| LTC2201IUK#PBF | LTC2201IUK#TRPBF | LTC2201UK | 48-Lead (7mm × 7mm) Plastic QFN | −40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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# CONVERTER CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution (No missing codes) | | | 16 | | | |
| Integral Linearity Error | Differential Analog Input (Note 5) | ● | | ±1.5 | ±5 | LSB |
| Differential Linearity Error | Differential Analog Input | ● | | ±0.3 | ±1 | LSB |
| Offset Error | (Note 6) | ● | | ±2 | ±10 | mV |
| Offset Drift | | | | ±10 | | µV/°C |
| Gain Error | External Reference | ● | | ±0.2 | ±1.5 | %FS |
| Full-Scale Drift | Internal Reference<br>External Reference | | | ±30<br>±15 | | ppm/°C<br>ppm/°C |
| Transition Noise | External Reference (2.5V Range, PGA = 0) | | | 1.92 | | LSB$_{RMS}$ |

# ANALOG INPUT
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Analog Input Range ($A_{IN}^+ - A_{IN}^-$) | $3.135V \leq V_{DD} \leq 3.465V$ | | | 1.667 or 2.5 | | $V_{P-P}$ |
| $V_{IN, CM}$ | Analog Input Common Mode | Differential Input (Note 7) | ● | 1 | 1.25 | 1.5 | V |
| $I_{IN}$ | Analog Input Leakage Current | $0V \leq A_{IN}^+, A_{IN}^- \leq V_{DD}$ (Note 9) | ● | −1 | | 1 | µA |
| $I_{SENSE}$ | SENSE Input Leakage Current | $0V \leq SENSE \leq V_{DD}$ (Note 10) | ● | −3 | | 3 | µA |
| $I_{MODE}$ | MODE Pin Pull-Down Current to GND | | | | 10 | | µA |
| $I_{\overline{OE}}$ | $\overline{OE}$ Pin Pull-Down Current to GND | | | | 10 | | µA |
| $C_{IN}$ | Analog Input Capacitance | Sample Mode CLK = 0<br>Hold Mode CLK = 0 | | | 10.5<br>1.4 | | pF<br>pF |
| $t_{AP}$ | Sample-and-Hold Acquisition Delay Time | | | | 0.9 | | ns |
| $t_{JITTER}$ | Sample-and-Hold Acquisition Delay Time Jitter | | | | 200 | | fs$_{RMS}$ |
| CMRR | Analog Input Common Mode Rejection Ratio | $1V < (A_{IN}^+ = A_{IN}^-) < 1.5V$ | | | 80 | | dB |
| BW-3dB | Full Power Bandwidth | $R_S < 20Ω$ | | | 380 | | MHz |

# DYNAMIC ACCURACY
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $A_{IN} = -1dBFS$. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SNR | Signal-to-Noise Ratio | 1MHz Input (2.25V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 81.6<br>79.4 | | dBFS<br>dBFS |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | ● | 80 | 81.6<br>79.4 | | dBFS<br>dBFS |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 81.4<br>79.3 | | dBFS<br>dBFS |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 80.8<br>78.9 | | dBFS<br>dBFS |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1 ) | | | 78.3<br>77.2 | | dBFS<br>dBFS |

# DYNAMIC ACCURACY The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $A_{IN} = -1dBFS$. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SFDR | Spurious Free Dynamic Range 2nd or 3rd Harmonic | 1MHz Input (2.5V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 100<br>100 | | dBc<br>dBc |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | ● | 85 | 100<br>100 | | dBc<br>dBc |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 95<br>100 | | dBc<br>dBc |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 90<br>95 | | dBc<br>dBc |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1) | | | 85<br>90 | | dBc<br>dBc |
| SFDR | Spurious Free Dynamic Range 4th Harmonic or Higher | 1MHz Input (2.5V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 100<br>100 | | dBc<br>dBc |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | ● | 90 | 100<br>100 | | dBc<br>dBc |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 100<br>100 | | dBc<br>dBc |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 100<br>100 | | dBc<br>dBc |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1) | | | 90<br>90 | | dBc<br>dBc |
| S/(N+D) | Signal-to-Noise Plus Distortion Ratio | 1MHz Input (2.5V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 81.5<br>79.3 | | dBFS<br>dBFS |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | ● | 79.7 | 81.5<br>79.3 | | dBFS<br>dBFS |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 81.3<br>79.2 | | dBFS<br>dBFS |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 80.6<br>78.6 | | dBFS<br>dBFS |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1) | | | 78.1<br>77 | | dBFS<br>dBFS |
| SFDR | Spurious Free Dynamic Range at −25dBFS Dither "OFF" | 1MHz Input (2.5V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 105<br>105 | | dBFS<br>dBFS |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | | | 105<br>105 | | dBFS<br>dBFS |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 105<br>105 | | dBFS<br>dBFS |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 105<br>105 | | dBFS<br>dBFS |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1) | | | 100<br>100 | | dBFS<br>dBFS |

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# DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $A_{IN}$ = −1dBFS. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SFDR | Spurious Free Dynamic Range at −25dBFS Dither "ON" | 1MHz Input (2.5V Range, PGA = 0)<br>1MHz Input (1.667V Range, PGA = 1) | | | 115<br>115 | | dBFS<br>dBFS |
| | | 5MHz Input (2.5V Range, PGA = 0)<br>5MHz Input (1.667V Range, PGA = 1) | | | 115<br>115 | | dBFS<br>dBFS |
| | | 12.5MHz Input (2.5V Range, PGA = 0)<br>12.5MHz Input (1.667V Range, PGA = 1) | | | 115<br>115 | | dBFS<br>dBFS |
| | | 30MHz Input (2.5V Range, PGA = 0)<br>30MHz Input (1.667V Range, PGA = 1) | | | 115<br>115 | | dBFS<br>dBFS |
| | | 70MHz Input (2.5V Range, PGA = 0)<br>70MHz Input (1.667V Range, PGA = 1) | | | 110<br>110 | | dBFS<br>dBFS |

# COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CM}$ Output Voltage | $I_{OUT}$ = 0 | 1.15 | 1.25 | 1.35 | V |
| $V_{CM}$ Output Tempco | $I_{OUT}$ = 0 | | ±40 | | ppm/°C |
| $V_{CM}$ Line Regulation | 3.135V ≤ $V_{DD}$ ≤ 3.465V | | 1 | | mV/V |
| $V_{CM}$ Output Resistance | 1mA ≤ | $I_{OUT}$ | ≤ 1mA | | 2 | | Ω |

# DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LOGIC INPUTS (CLK, OE, DITH, PGA, SHDN, RAND)** | | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}$ = 3.3V | | ● | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD}$ = 3.3V | | ● | | | 0.8 | V |
| $I_{IN}$ | Digital Input Current | $V_{IN}$ = 0V to $V_{DD}$ | | ● | | | ±10 | μA |
| $C_{IN}$ | Digital Input Capacitance | (Note 7) | | | | 1.5 | | pF |
| **LOGIC OUTPUTS** | | | | | | | | |
| **$OV_{DD}$ = 3.3V** | | | | | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = −10μA<br>$I_O$ = −200μA | ● | 3.1 | 3.299<br>3.29 | | V<br>V |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = 160μA<br>$I_O$ = 1.6mA | ● | | 0.01<br>0.10 | 0.4 | V<br>V |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | | −50 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = 3.3V | | | | 50 | | mA |
| **$OV_{DD}$ = 2.5V** | | | | | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = −200μA | | | 2.49 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = 1.60mA | | | 0.1 | | V |
| **$OV_{DD}$ = 1.8V** | | | | | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = −200μA | | | 1.79 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}$ = 3.3V | $I_O$ = 1.60mA | | | 0.1 | | V |

# LTC2201

## POWER REQUIREMENTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $A_{IN}$ = −1dBFS. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--------|-----------|------------|---|-----|-----|-----|-------|
| $V_{DD}$ | Analog Supply Voltage | | ● | 3.135 | 3.3 | 3.465 | V |
| $P_{SHDN}$ | Shutdown Power | SHDN = $V_{DD}$, CLK = $V_{DD}$ | | | 2 | | mW |
| $OV_{DD}$ | Output Supply Voltage | | ● | 0.5 | | 3.6 | V |
| $I_{VDD}$ | Analog Supply Current | | ● | | 64 | 80 | mA |
| $P_{DIS}$ | Power Dissipation | | ● | | 211 | 264 | mW |

## TIMING CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 4)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--------|-----------|------------|---|-----|-----|-----|-------|
| $f_S$ | Sampling Frequency | | ● | 1 | | 20 | MHz |
| $t_L$ | CLK Low Time | Duty Cycle Stabilizer Off<br>Duty Cycle Stabilizer On | ●<br>● | 20<br>5 | 25<br>25 | 500<br>500 | ns<br>ns |
| $t_H$ | CLK High Time | Duty Cycle Stabilizer Off<br>Duty Cycle Stabilizer On | ●<br>● | 20<br>5 | 25<br>25 | 500<br>500 | ns<br>ns |
| $t_{AP}$ | Sample-and-Hold Aperture Delay | | | | 0.9 | | ns |
| $t_D$ | CLK to DATA Delay | $C_L$ = 5pF (Note 7) | ● | 1.3 | 3.1 | 4.9 | ns |
| $t_C$ | CLK to CLKOUT Delay | $C_L$ = 5pF (Note 7) | ● | 1.3 | 3.1 | 4.9 | ns |
| $t_{SKEW}$ | DATA to CLKOUT Skew | $C_L$ = 5pF (Note 7) | ● | −0.6 | 0 | 0.6 | ns |
| | DATA Access Time<br>Bus Relinquish Time | $C_L$ = 5pF (Note 7)<br>(Note 7) | ●<br>● | | 5<br>5 | 15<br>15 | ns<br>ns |
| | Pipeline Latency | | | | 7 | | Cycles |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND, with GND and OGND shorted (unless otherwise noted).

**Note 3:** When these pin voltages are taken below GND or above $V_{DD}$, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above $V_{DD}$ without latchup.

**Note 4:** $V_{DD}$ = 3.3V, $f_{SAMPLE}$ = 20MHz, input range = 2.5$V_{P-P}$ with differential drive (PGA = 0), unless otherwise specified.

**Note 5:** Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

**Note 6:** Offset error is the offset voltage measured from −1/2LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** Recommended operating conditions.

**Note 9:** Dynamic current from switched capacitor inputs is large compared to DC leakage current, and will vary with sample rate.

**Note 10:** Leakage current will experience transient at power up. Keep resistance < 1kΩ.
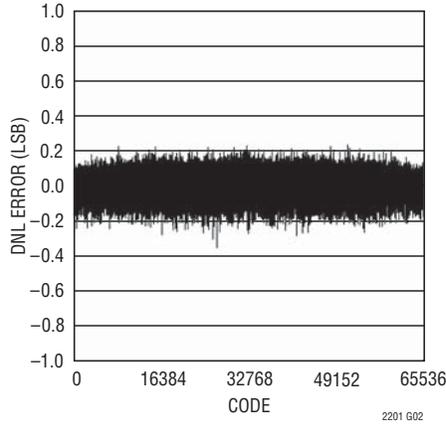
LINEAR TECHNOLOGY

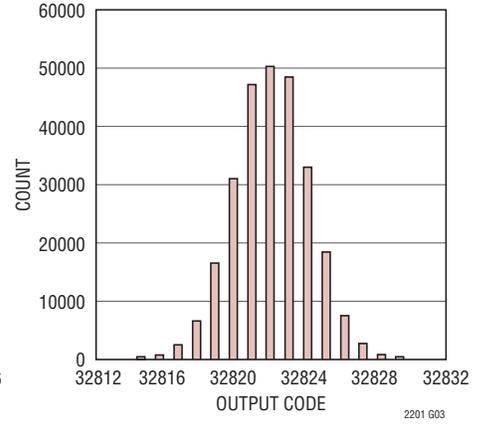# TIMING DIAGRAM
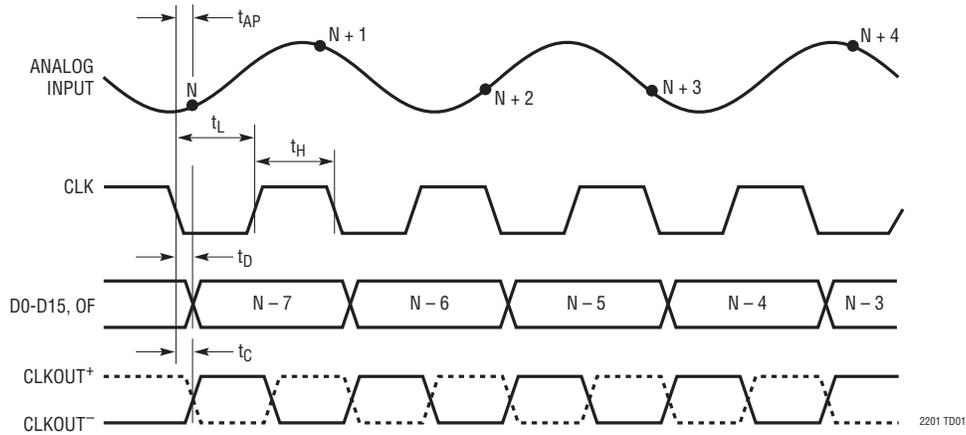


# TYPICAL PERFORMANCE CHARACTERISTICS
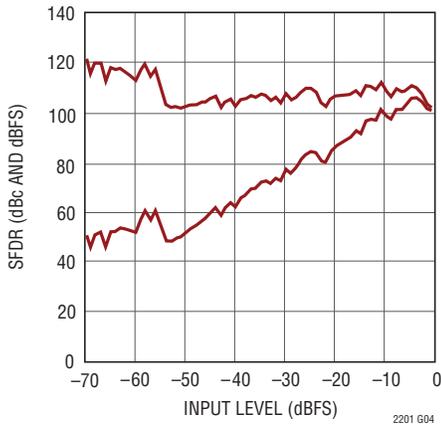
**Integral Nonlinearity (INL) vs Output Code**
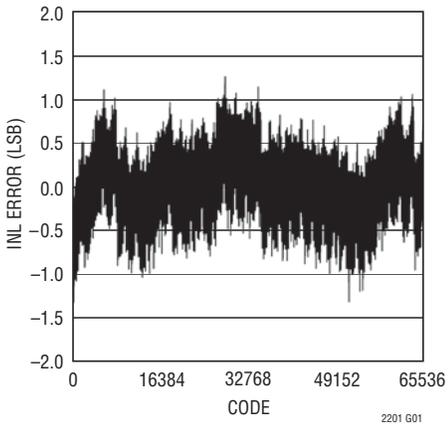


**Differential Nonlinearity (DNL) vs Output Code**
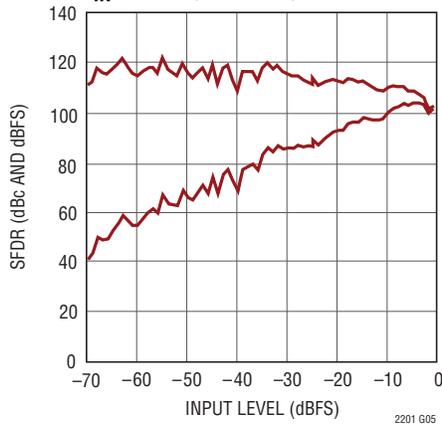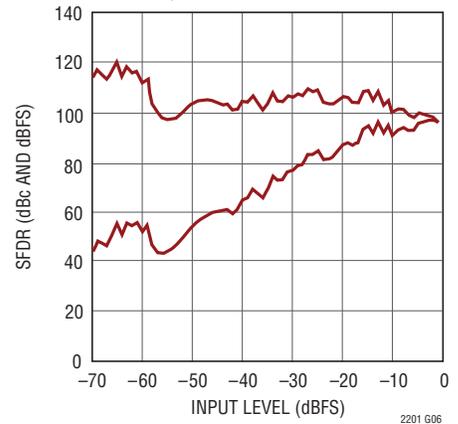


**AC Grounded Input Histogram (256k Samples)**



**SFDR vs Input Level, $f_{IN}$ = 5MHz, PGA = 0, Dither "Off"**
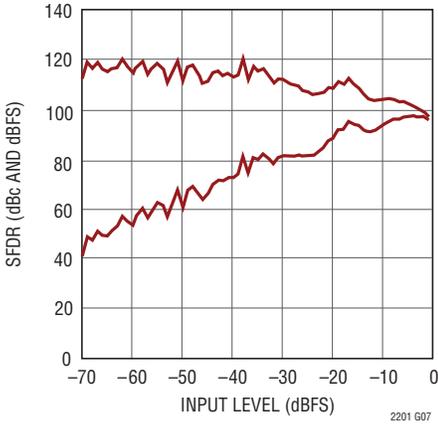


**SFDR vs Input Level, $f_{IN}$ = 5MHz, PGA = 0, Dither "On"**



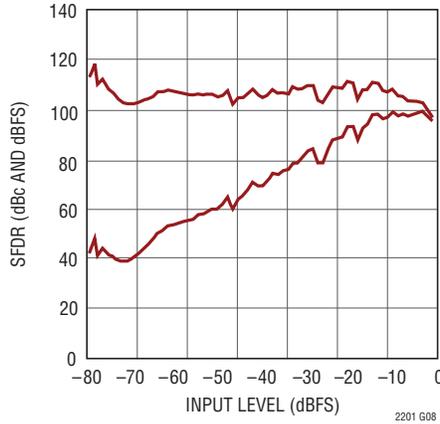**SFDR vs Input Level, $f_{IN}$ = 12.7MHz, PGA = 0, Dither "Off"**
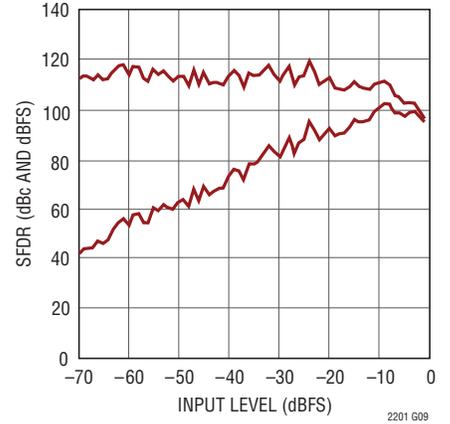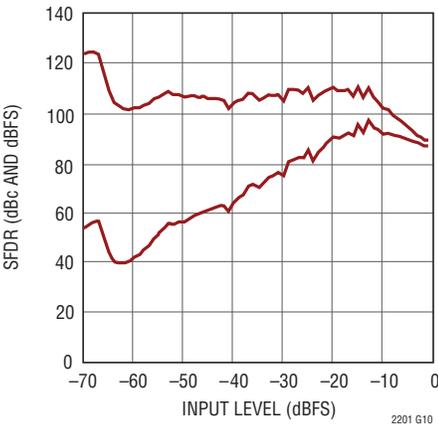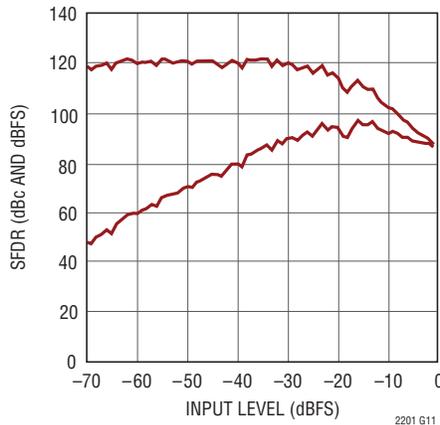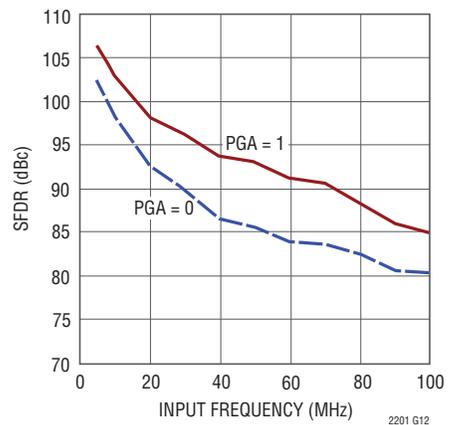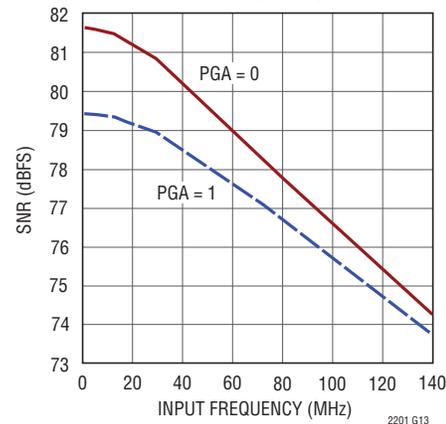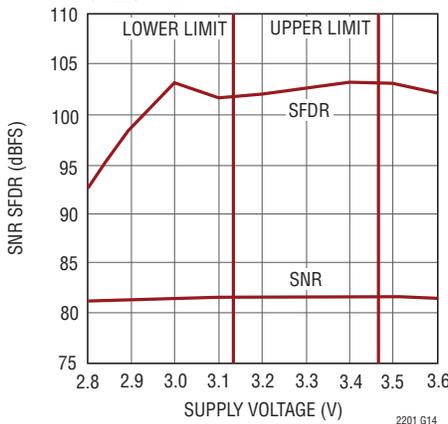
# TYPICAL PERFORMANCE CHARACTERISTICS

**SFDR vs Input Level, $f_{IN}$ = 12.7MHz, PGA = 0, Dither "On"**



2201 G07

**SFDR vs Input Level, $f_{IN}$ = 30.1MHz, PGA = 0, Dither "Off"**



2201 G08

**SFDR vs Input Level, $f_{IN}$ = 30.1MHz, PGA = 0, Dither "On"**



2201 G09

**SFDR vs Input Level, $f_{IN}$ = 70.1MHz, PGA = 0, Dither "Off"**



2201 G10

**SFDR vs Input Level, $f_{IN}$ = 70.1MHz, PGA = 0, Dither "On"**



2201 G11

**SFDR (HD2 or HD3) vs Input Frequency**



2201 G12

**SNR vs Input Frequency**



2201 G13

**SNR and SFDR vs Supply Voltage ($V_{DD}$), $f_{IN}$ = 5MHz**



2201 G14

**$I_{VDD}$ vs Sample Rate, 5MHz Sine Wave, –1dBFS**



2201 G15

2201f

8
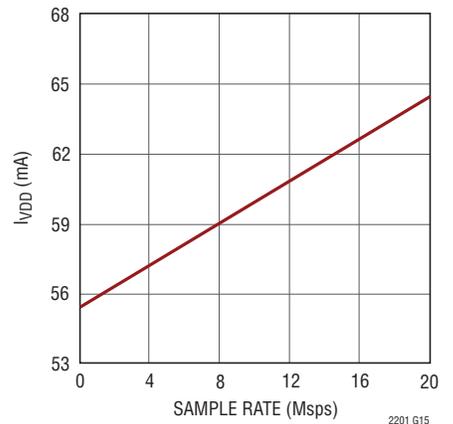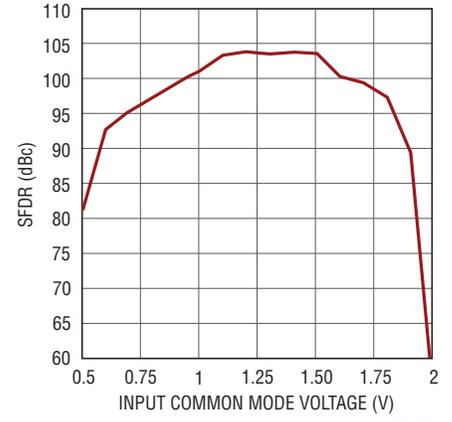
# TYPICAL PERFORMANCE CHARACTERISTICS

**Normalized Full Scale
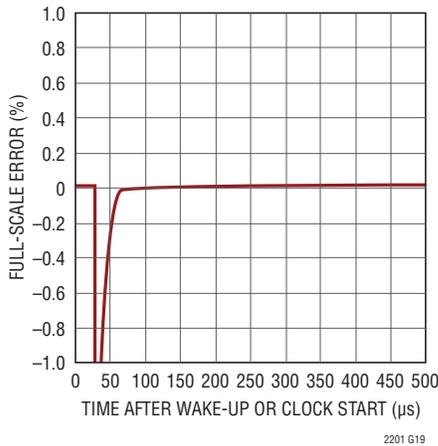vs Temperature, Internal
Reference, 5 Units**



2201 G16
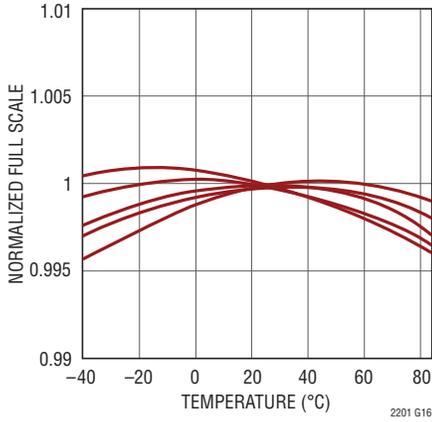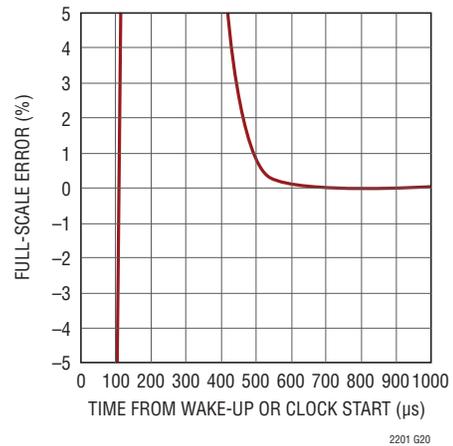
**Offset Voltage
vs Temperature, 5 Units**



2201 G17
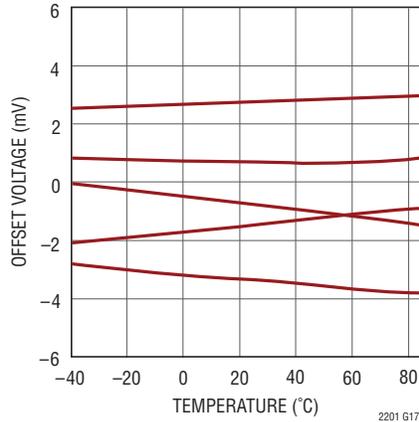
**SFDR vs Input Common Mode
Voltage, $f_{IN}$ = 5MHz, −1dBFS,
PGA = 0**



2201 G18

**Mid-Scale Settling After Wake
Up from Shutdown or Starting
Encode Clock**



2201 G19

**Full-Scale Settling After Wake
Up from Shutdown or Starting
Encode Clock**



2201 G20

# PIN FUNCTIONS

**SENSE (Pin 1):** Reference Mode Select and External Reference Input. Tie SENSE to $V_{DD}$ with 1k $\Omega$ or less to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.5V (PGA = 0).

**$V_{CM}$ (Pin 2):** 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2µF. Ceramic chip capacitors are recommended.

**$V_{DD}$ (Pins 3, 4, 12, 13, 14):** 3.3V Analog Supply Pin. Bypass to GND with 0.1µF ceramic chip capacitors.

**GND (Pins 5, 8, 9, 11, 15, 48, 49):** ADC Power Ground.

**$A_{IN}^+$ (Pin 6):** Positive Differential Analog Input.

**$A_{IN}^-$ (Pin 7):** Negative Differential Analog Input.

**CLK (Pin 10):** Clock Input. The hold phase of the sample-and-hold circuit begins on the falling edge. The output data may be latched on the rising edge of CLK.

**SHDN (Pin 16):** Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

**DITH (Pin 17):** Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

**D0-D15 (Pins 18-22, 26-28, 32-35 and 39-42):** Digital Outputs. D15 is the MSB.

**OGND (Pins 23, 31 and 38):** Output Driver Ground.

**$OV_{DD}$ (Pins 24, 25, 36, 37):** Positive Supply for the Output Drivers. Bypass to ground with 0.1µF capacitors.

**CLKOUT⁻ (Pin 29):** Data Valid Output. CLKOUT⁻ will toggle at the sample rate. Latch the data on the falling edge of CLKOUT⁻.

**CLKOUT⁺ (Pin 30):** Inverted Data Valid Output. CLKOUT⁺ will toggle at the sample rate. Latch the data on the rising edge of CLKOUT⁺.

**OF (Pin 43):** Over/Under Flow Digital Output. OF is high when an over or under flow has occurred.

**$\overline{OE}$ (Pin 44):** Output Enable Pin. Low enables the digital output drivers. High puts digital outputs in Hi-Z state.

**MODE (Pin 45):** Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3$V_{DD}$ selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3$V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to $V_{DD}$ selects 2's complement output format and disables the clock duty cycle stabilizer.

**RAND (Pin 46):** Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. The mode of operation reduces the effects of digital output interference.

**PGA (Pin 47):** Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of 2.5$V_{P-P}$. High selects a front-end gain of 1.5, input range of 1.667$V_{P-P}$.

**GND (Exposed Pad, Pin 49):** ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.
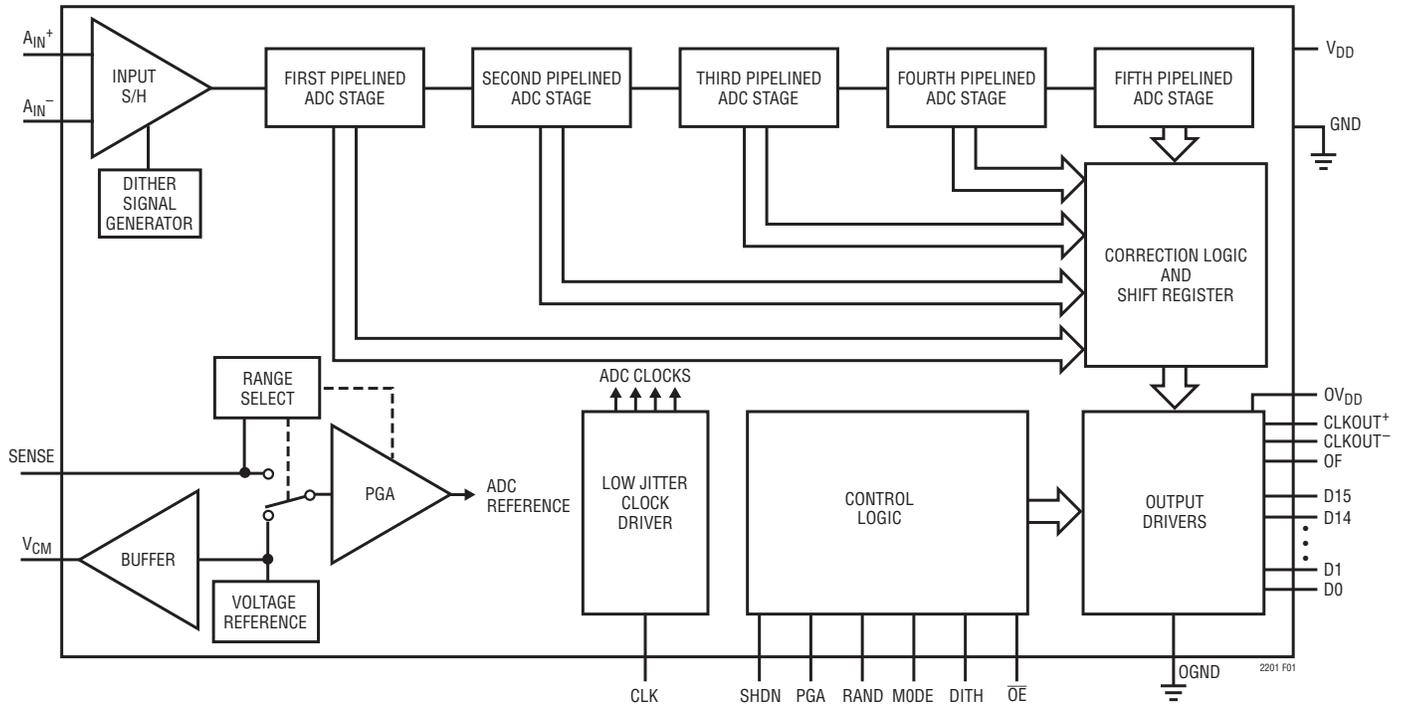
# BLOCK DIAGRAM



**Figure 1. Functional Block Diagram**

# APPLICATIONS INFORMATION

## DYNAMIC PERFORMANCE

### Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

### Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

### Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\left(\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... V_N^2)}/V_1\right)$$

where $V_1$ is the RMS amplitude of the fundamental frequency and $V_2$ through $V_N$ are the amplitudes of the second through nth harmonics.

### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa - fb) and (fa - 2fb). The 3rd order IMD is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

### Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

### Full Power Bandwidth

The Full Power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

### Aperture Delay Time

The time from when CLK reaches 0.45 of $V_{DD}$ to the instant that the input signal is held by the sample-and-hold circuit.

### Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\left(2\pi \bullet f_{IN} \bullet t_{JITTER}\right)$$

# APPLICATIONS INFORMATION

## CONVERTER OPERATION

The LTC2201 is a CMOS pipelined multistep converter with a front-end PGA. As shown in Figure 1, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample-and-hold circuit.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

The phase of operation is determined by the state of the CLK input pin.

When CLK is high, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "input S/H" shown in the block diagram. At the instant that CLK transitions from high to low, the voltage on the sample capacitors is held. While CLK is low, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the low phase of CLK. When CLK goes back high, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes low, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being sent to the output buffer.

## SAMPLE/HOLD OPERATION AND INPUT DRIVE

### Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2201 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors ($C_{SAMPLE}$) through NMOS transitors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.
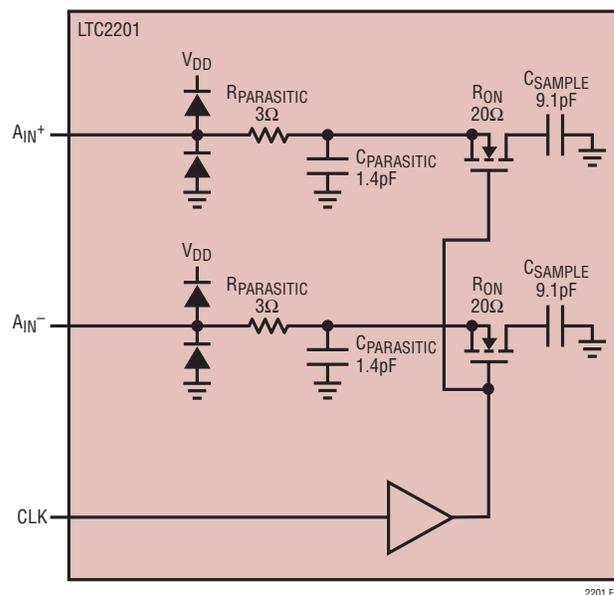


**Figure 2. Equivalent Input Circuit**

During the sample phase when CLK is high, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When CLK transitions from high to low, the sampled input voltage is held on the sampling capacitors. During the hold phase when CLK is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As CLK transitions from low to high, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time at the input of the converter. If the change between the last sample and

# APPLICATIONS INFORMATION

the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

## Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input may swing ±0.625V for the 2.5V range (PGA = 0) or ±0.417V for the 1.667V range (PGA = 1), around a common mode voltage of 1.25V. The $V_{CM}$ output pin (Pin 2) is designed to provide the common mode bias level. $V_{CM}$ can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The $V_{CM}$ pin must be bypassed to ground close to the ADC with 2.2µF or greater.

## Input Drive Impedence

As with all high performance, high speed ADCs the dynamic performance of the LTC2201 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the rising edge of CLK the sample and hold circuit will connect the 9.1pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when CLK falls, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{CLK})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

## INPUT DRIVE CIRCUITS

Figure 3 shows the LTC2201 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with $V_{CM}$, setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns

ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50Ω can reduce the input bandwidth and increase high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.
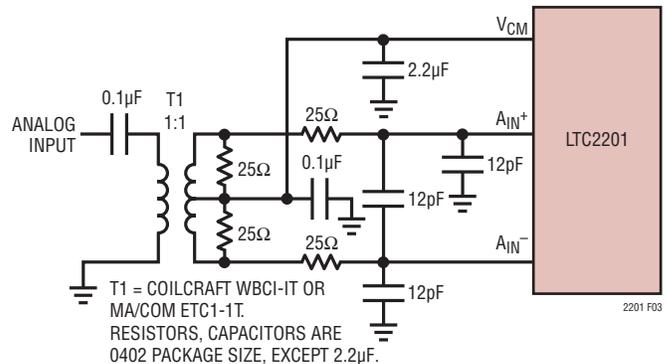


**Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 1MHz to 100MHz**

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

Figure 4 shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high frequency response and balance than flux coupled center tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.25V.
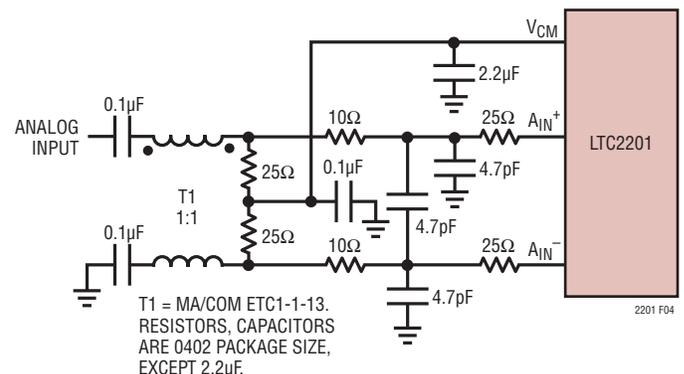


**Figure 4. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 50MHz to 250MHz**

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# APPLICATIONS INFORMATION

Figure 5 demonstrates the use of an LTC1994 differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp will limit the SFDR at high input frequencies.
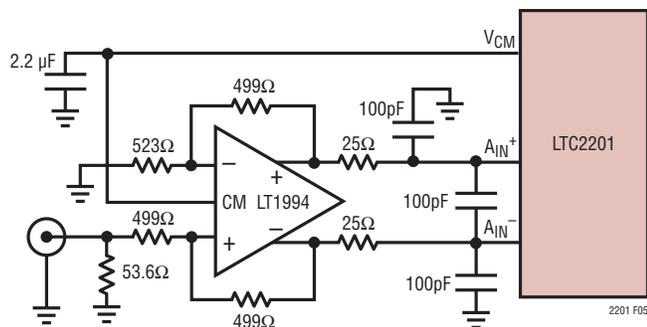


**Figure 5. DC Coupled Input with Differential Amplifier**

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input.

## Reference Operation

Figure 6 shows the LTC2201 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2201 has three modes of reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to $V_{DD}$. To use the external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full scale range of $2.5V_{P-P}$ (PGA = 0). A 1.25V output, $V_{CM}$, is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the $V_{CM}$ output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; it will not be stable without this capacitor. The minimum value required for stability is 2.2μF.

The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and is not accessible for external use.
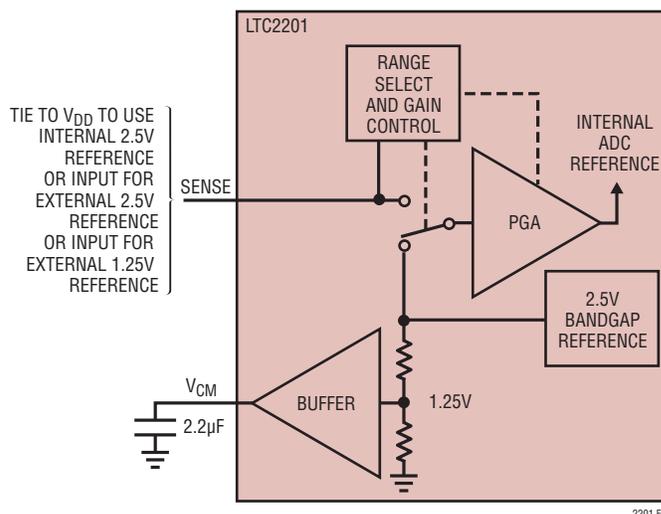


**Figure 6. Reference Circuit**

The SENSE pin can be driven ±5% around the nominal 2.5V or 1.25V external reference input. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to $V_{DD}$ as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with at least a 1μF ceramic capacitor.
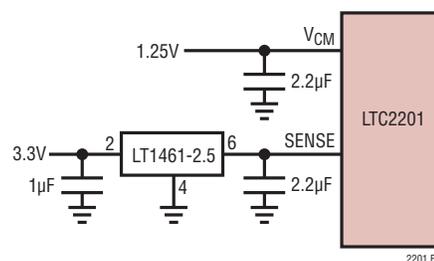


**Figure 7. A 2.5V Range ADC
with an External 2.5V Reference**

# APPLICATIONS INFORMATION

**PGA Pin**

The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of $2.5V_{P-P}$; PGA = 1 selects an input range of $1.667V_{P-P}$. The 2.5V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 2.4dB worse. See the Typical Performance Characteristics section.

**Driving the Clock Input**

The CLK input can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low-jitter squaring circuit before the CLK pin (Figure 8).
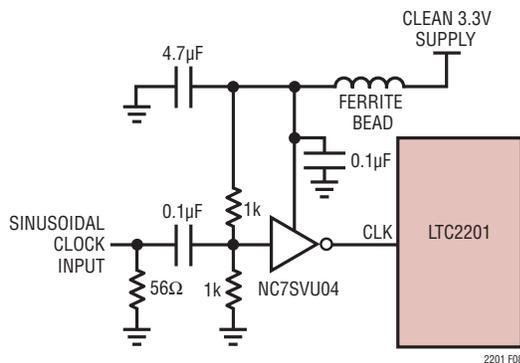


**Figure 8. Sinusoidal Single-Ended CLK Drive**

The noise performance of the LTC2201 can depend on the clock signal quality as much as on the analog input. Any noise present on the clock signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical, such as when digitizing high input frequencies, use as large an amplitude as possible. It is also helpful to drive the CLK pin with a low-jitter high frequency source which has been divided down to the appropriate sample rate. If the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

**Maximum and Minimum Conversion Rates**

The maximum conversion rate for the LTC2201 is 20Msps. For the ADC to operate properly the CLK signal should have a 50% (±10%) duty cycle. Each half cycle must have at least 20ns for the LTC2201 internal circuitry to have enough settling time for proper operation.

An on-chip clock duty cycle stabilizer may be activated if the input clock does not have a 50% duty cycle. This circuit uses the falling edge of CLK pin to sample the analog input. The rising edge of CLK is ignored and an internal rising edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2201 sample rate is determined by droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2201 is 1Msps.

# APPLICATIONS INFORMATION

## DIGITAL OUTPUTS

### Digital Output Buffers

Figure 9 shows an equivalent circuit for a single output buffer in CMOS Mode. Each buffer is powered by $OV_{DD}$ and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as $50\Omega$ to external circuitry and eliminates the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2201 should drive a small capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as a ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of $43\Omega$ on chip.

Lower $OV_{DD}$ voltages will also help reduce interference from the digital outputs.
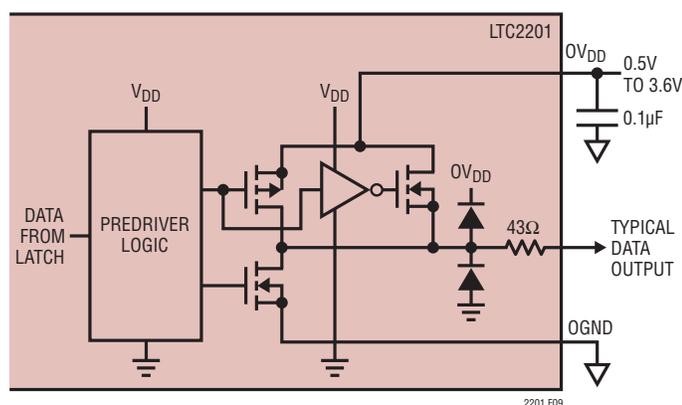


**Figure 9. Equivalent Circuit for a Digital Output Buffer**

## Data Format

The LTC2201 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and $V_{DD}$. An external resistor divider can be user to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 1 shows the logic states for the MODE pin.

**Table 1. MODE Pin Function**

| MODE | OUTPUT FORMAT | CLOCK DUTY CYCLE STABILIZER |
|---|---|---|
| 0(GND) | Offset Binary | Off |
| $1/3V_{DD}$ | Offset Binary | On |
| $2/3V_{DD}$ | 2's Complement | On |
| $V_{DD}$ | 2's Complement | Off |

## Overflow Bit

An overflow output bit (OF) indicates when the converter is over-ranged or under-ranged. A logic high on the OF pin indicates an overflow or underflow.

## Output Clock

The ADC has a delayed version of the CLK input available as a digital output. Both a noninverted version, CLKOUT⁺ and an inverted version CLKOUT⁻ are provided. The CLKOUT⁺/CLKOUT⁻ can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal clock. Data can be latched on the rising edge of CLKOUT⁺ or the falling edge of CLKOUT⁻. CLKOUT⁺ falls and CLKOUT⁻ rises as the data outputs are updated.

# APPLICATIONS INFORMATION

## Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is "Randomized" by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT output are not affected. The output Randomizer function is active when the RAND pin is high.
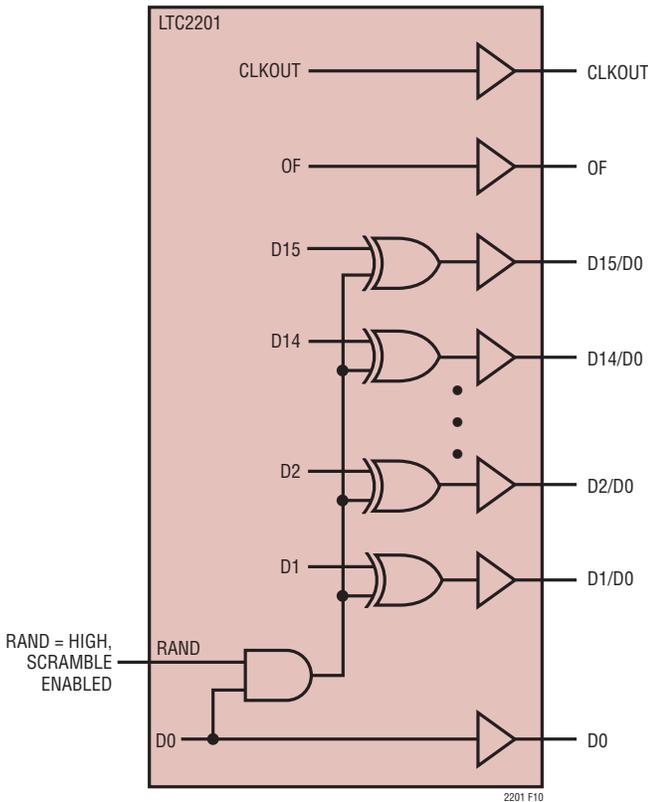
## Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, $OV_{DD}$, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then $OV_{DD}$ should be tied to that same 1.8V supply. In CMOS mode $OV_{DD}$ can be powered with any logic voltage up to 3.6V. OGND can be powered with any voltage from ground up to 1V and must be less than $OV_{DD}$. The logic outputs will swing between OGND and $OV_{DD}$.
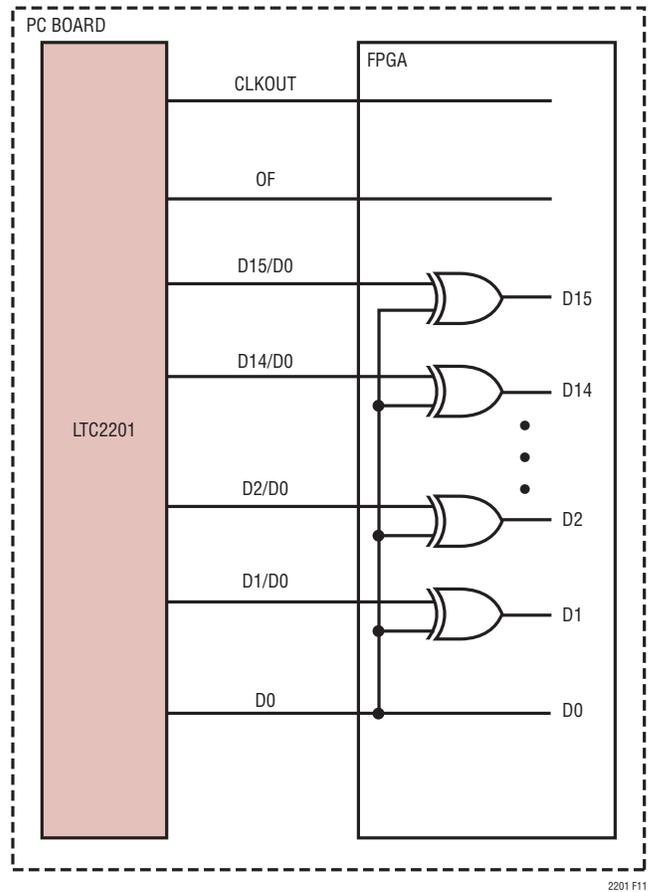


**Figure 11. Descrambling a Scrambled Digital Output**



**Figure 10. Functional Equivalent of Digital Output Randomizer**

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# APPLICATIONS INFORMATION

## Internal Dither

The LTC2201 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input's location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

As shown in Figure 12, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC is calibrated to result in less than 0.5dB elevation in the noise floor of the ADC, as compared to the noise floor with dither off.
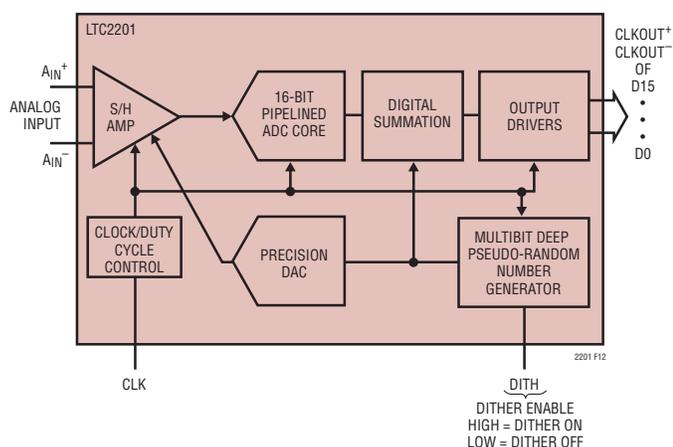


**Figure 12. Functional Equivalent Block Diagram of Internal Dither Circuit**

## Grounding and Bypassing

The LTC2201 require a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTC2201 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the $V_{DD}$, $V_{CM}$, and $OV_{DD}$ pins. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2201 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

## Heat Transfer

Most of the heat generated by the LTC2201 is transferred from the die through the bottom-side exposed pad. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. It is critical that the exposed pad and all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

# APPLICATIONS INFORMATION

**Evaluation Circuit Schematic of the LTC2201**
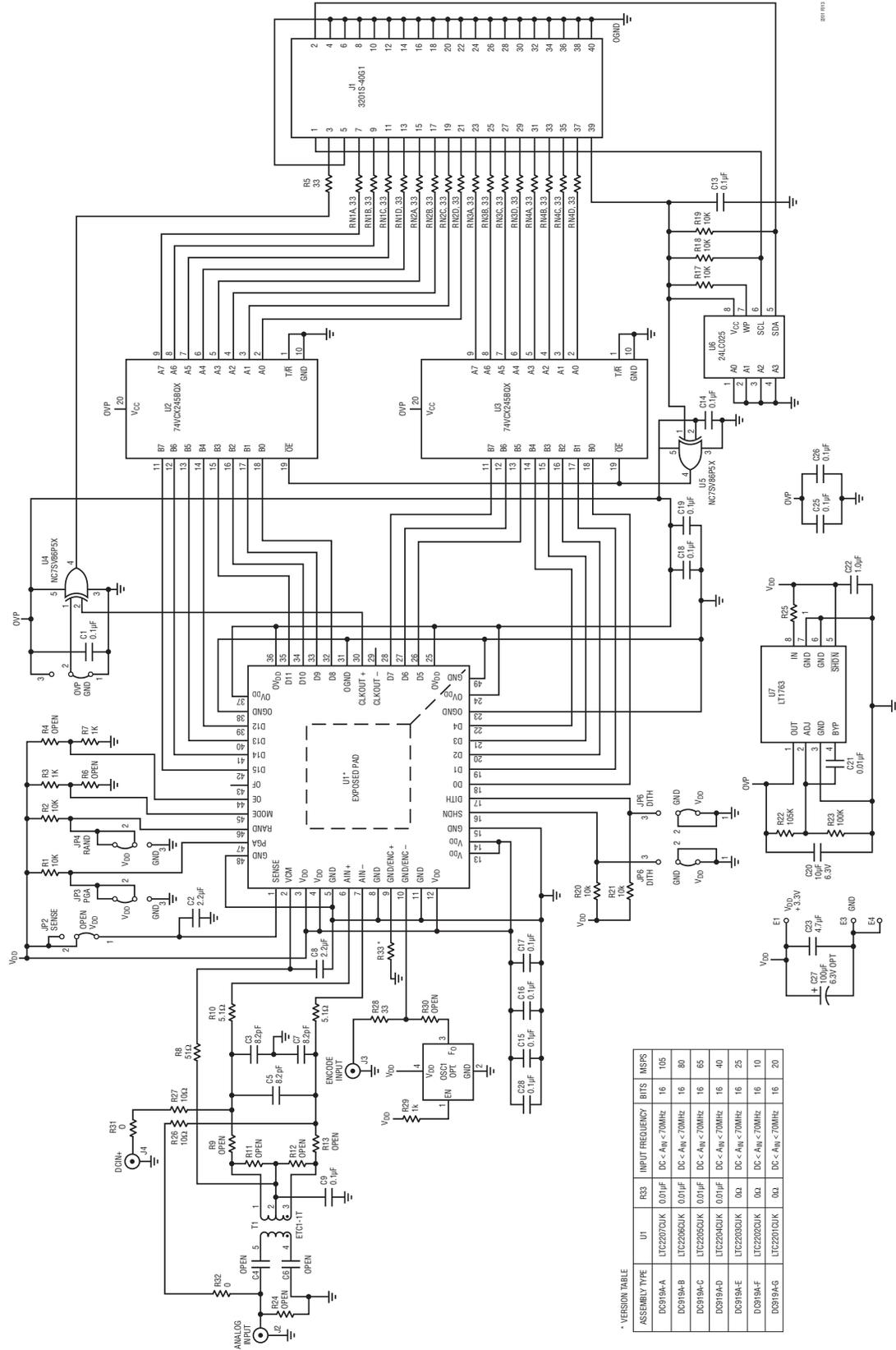


| * VERSION TABLE | | | | | |
|---|---|---|---|---|---|
| ASSEMBLY TYPE | U1 | R33 | INPUT FREQUENCY | BITS | MSPS |
| DC919A-A | LTC2207CUJK | 0.01µF | DC < A_IN < 70MHz | 16 | 105 |
| DC919A-B | LTC2206CUJK | 0.01µF | DC < A_IN < 70MHz | 16 | 80 |
| DC919A-C | LTC2205CUJK | 0.01µF | DC < A_IN < 70MHz | 16 | 65 |
| DC919A-D | LTC2204CUJK | 0.01µF | DC < A_IN < 70MHz | 16 | 40 |
| DC919A-E | LTC2203CUJK | 0Ω | DC < A_IN < 70MHz | 16 | 25 |
| DC919A-F | LTC2202CUJK | 0Ω | DC < A_IN < 70MHz | 16 | 10 |
| DC919A-G | LTC2201CUJK | 0Ω | DC < A_IN < 70MHz | 16 | 20 |

# APPLICATIONS INFORMATION
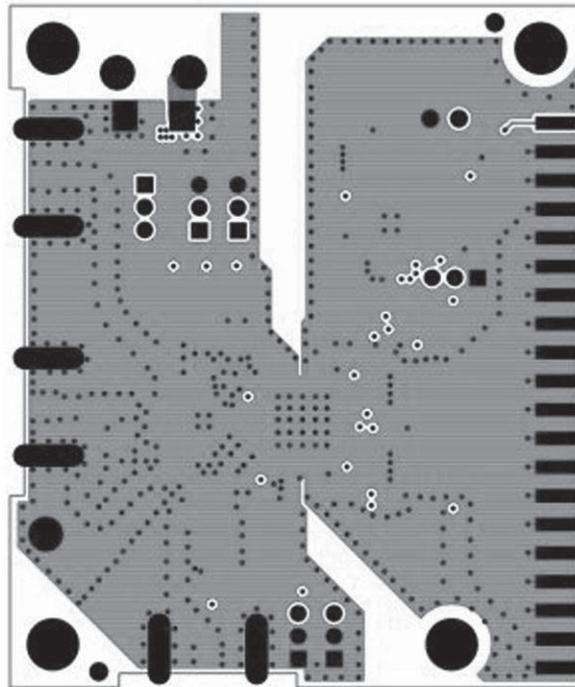
**Silkscreen Top**



**Inner Layer 2**
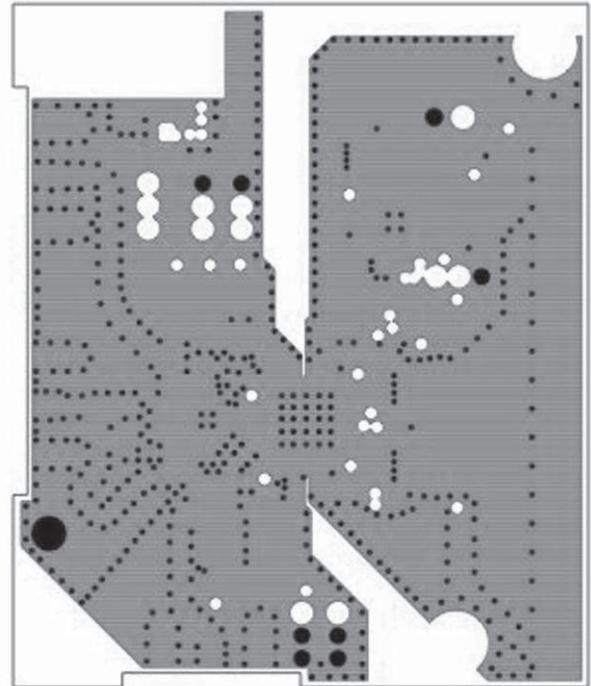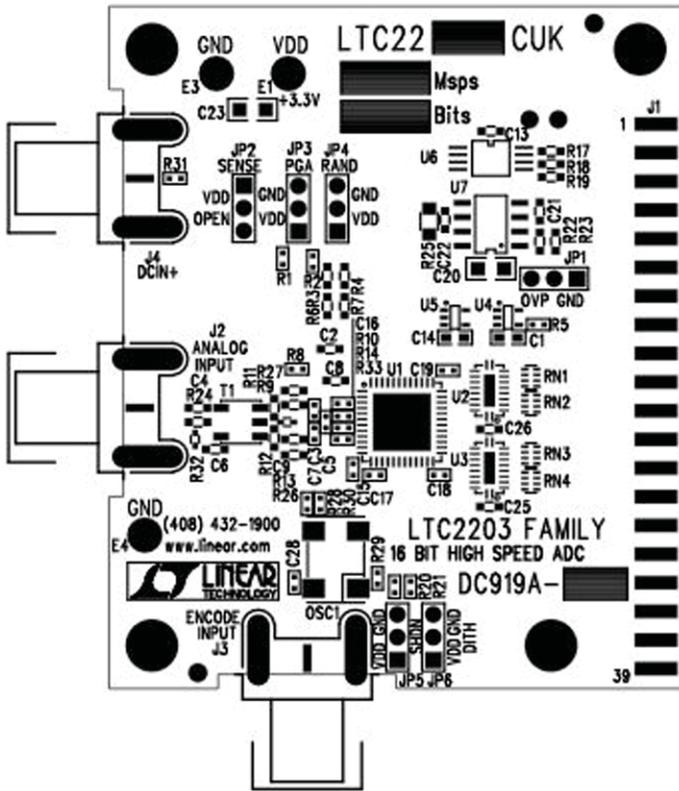


**Silkscreen Topside**



**Inner Layer 3**
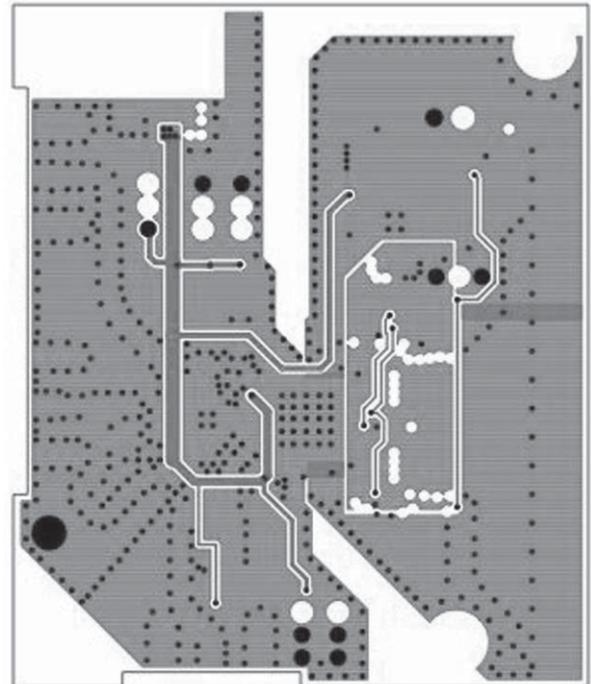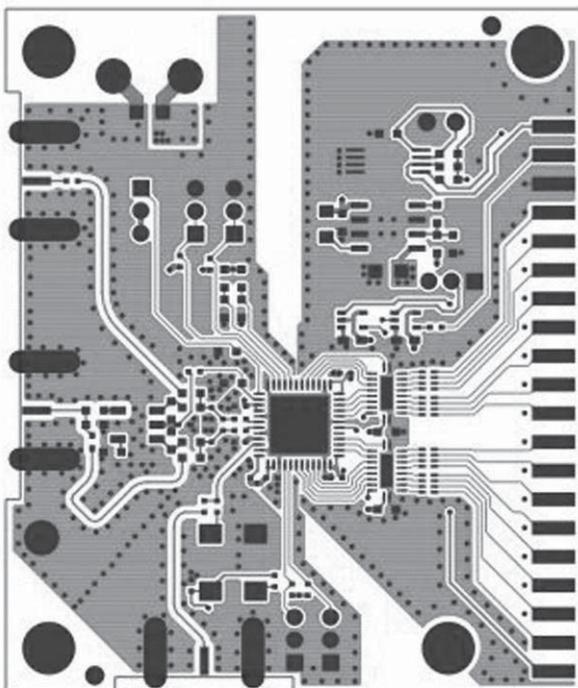
# APPLICATIONS INFORMATION

**Silkscreen Bottom Side**

**Silkscreen Bottom**

LTC CONFIDENTIAL— FOR CUSTOMER USE ONLY

C27
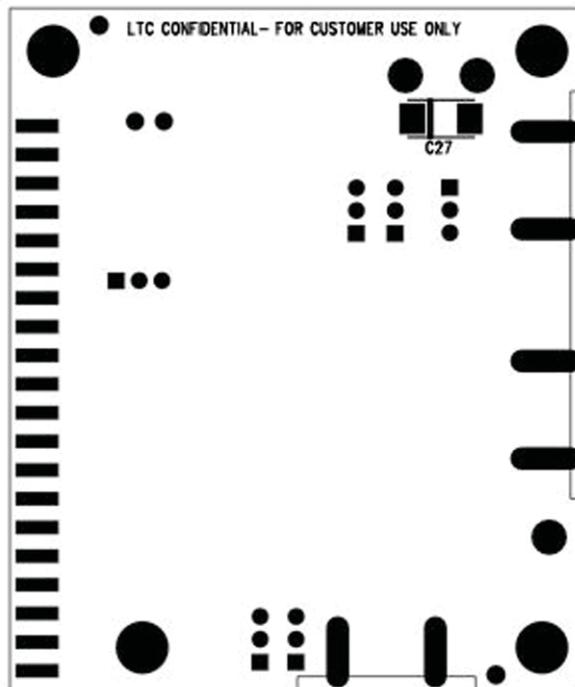
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UK Package**
**48-Lead Plastic QFN (7mm × 7mm)**
(Reference LTC DWG # 05-08-1704 Rev C)

0.70 ±0.05

5.15 ± 0.05

5.50 REF
(4 SIDES)

6.10 ±0.05   7.50 ±0.05

5.15 ± 0.05

PACKAGE OUTLINE

0.25 ±0.05
0.50 BSC
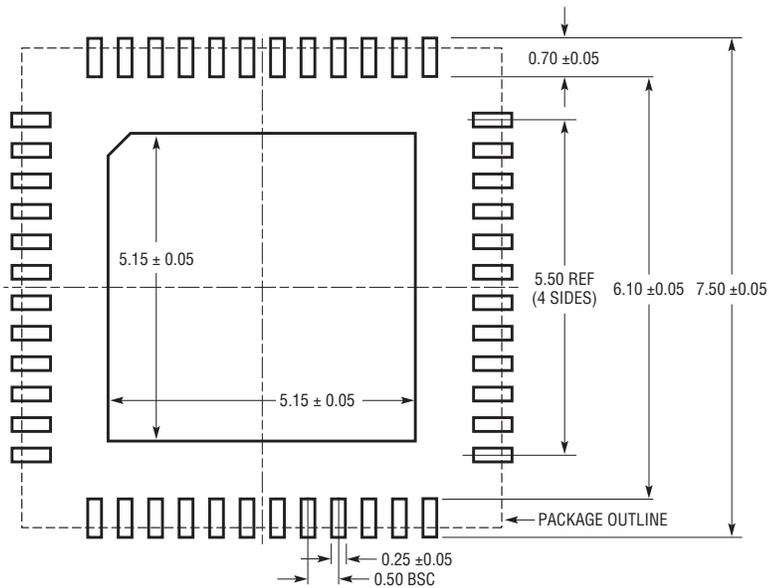
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

7.00 ± 0.10
(4 SIDES)

0.75 ±0.05

R = 0.10
TYP

R = 0.115
TYP

47   48

0.40 ± 0.10

1

2

PIN 1 TOP MARK
(SEE NOTE 6)

PIN 1
CHAMFER
C = 0.35

5.50 REF
(4-SIDES)

5.15 ± 0.10

5.15 ± 0.10

0.200 REF

0.00 – 0.05

(UK48) QFN 0406 REV C

0.25 ± 0.05
0.50 BSC

BOTTOM VIEW—EXPOSED PAD
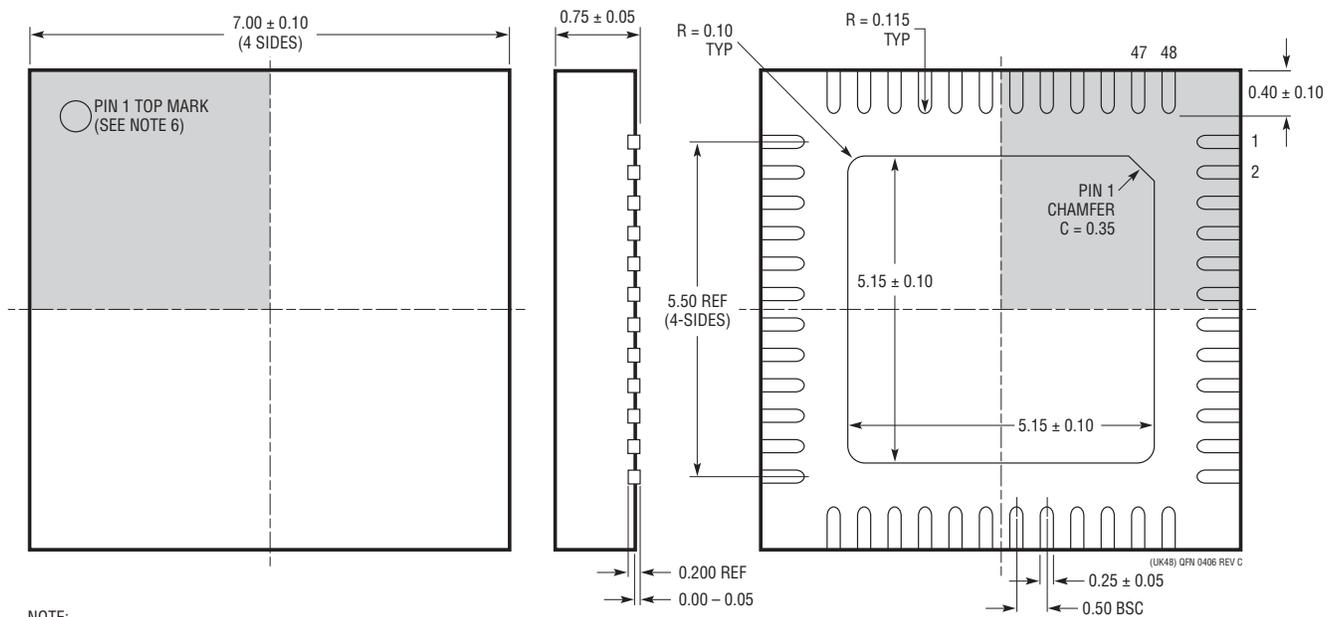
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC2202 | 16-Bit, 10Msps, 3.3V ADC | 140mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC2203 | 16-Bit, 25Msps, 3.3V ADC | 220mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC6404-1 | 600MHz Low Noise, Low Distortion, Differential ADC Driver | 1.5nV/$\sqrt{Hz}$ Noise, −90dBc Distortion at 10MHz |
| LT1994 | Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver | Low Distortion: −94dBc at 1MHz |
| LTC2204 | 16-Bit, 40Msps, 3.3V ADC | 480mW, 79.1dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC2205 | 16-Bit, 65Msps, 3.3V ADC | 610mW, 79dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC2206 | 16-Bit, 80Msps, 3.3V ADC | 725mW, 77.9dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC2207 | 16-Bit, 105Msps, 3.3V ADC | 900mW, 77.9dB SNR, 100dB SFDR, 48-Pin QFN |
| LTC2208 | 16-Bit, 130Msps, 3,3V ADC, LVDS Outputs | 1250mW, 77.1dB SNR, 100dB SFDR, 64-Pin QFN |
| LTC2224 | 12-Bit, 135Msps, 3.3V ADC, High IF Sampling | 630mW, 67.6dB SNR, 84dB SFDR, 48-Pin QFN |
| LTC2242-12 | 12-Bit, 250Msps, 2.5V ADC, LVDS Outputs | 740mW, 65.4dB SNR, 84dB SFDR, 64-Pin QFN |
| LTC2255 | 14-Bit, 125Msps, 3V ADC, Lowest Power | 395mW, 72.5dB SNR, 88dB SFDR, 32-Pin QFN |
| LTC2284 | 14-Bit, Dual, 105Msps, 3V ADC, Low Crosstalk | 540mW, 72.4dB SNR, 88dB SFDR, 64-pin QFN |
| LT5512 | DC-3GHz High Signal Level Downconverting Mixer | DC to 3GHz, 21dBm IIP3, Integrated LO Buffer |
| LT5514 | Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain | 450MHz to 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step |
| LT5515 | 1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator | High IIP3: 20dBm at 1.9GHz, Integrated LO Quadrature Generator |
| LT5516 | 800MHz to 1.5GHz Direct Conversion Quadrature Demodulator | High IIP3: 21.5dBm at 900MHz, Integrated LO Quadrature Generator |
| LT5517 | 40MHz to 900MHz Direct Conversion Quadrature Demodulator | High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator |
| LT5522 | 600MHz to 2.7GHz High Linearity Downconverting Mixer | 4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz. NF = 12.5dB, 50Ω Single Ended RF and LO Ports |