19-0040; Rev 0; 6/92

EVALUATION KIT AVAILABLE

MAXIM

Palmtop Computer and LCD Power-Supply Regulators

MAX722/MAX723

General Description

The MAX722 and MAX723 CMOS power-supply ICs create dual regulated DC outputs for small, battery-operated microprocessor systems. Each device generates a main output (3V or 5V, selectable) and a negative auxiliary output that is adjustable for LCDs. Each device accepts two input voltages. Power can come from a main battery (two or three alkaline or NiCad), or an unregulated DC source such as an AC-DC wall adapter.

The MAX722/MAX723 provide three improvements over prior-art devices. Physical size is reduced; the high switching frequencies (up to 0.5MHz), made possible by MOSFET power transistors, allow for tiny (<5mm diameter) surface-mount magnetics. Efficiency is also improved to 87% (10% better than with low-voltage regulators made in bipolar technology). And supply current is reduced to 60µA by CMOS construction and a unique constant-off-time pulse-frequency modulation (PFM) control scheme.

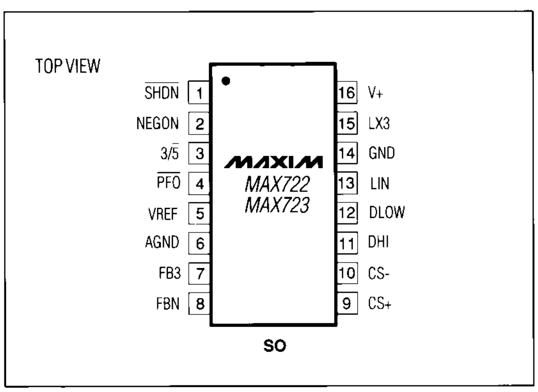
The MAX722 and MAX723 differ only in the lower fixed output voltage of the main regulator, with a 3.3V output for the MAX722 and a 3.0V output for the MAX723.

For flash memory or PCMCIA applications that require a +12V output voltage, refer to the MAX717-721 data sheet.

Applications

Palmtop Computers
LCD Contrast Control
Portable Data-Collection Equipment
Portable Data Communicators
Medical Instrumentation
Bar-Code Scanners

Pin Configuration



Features

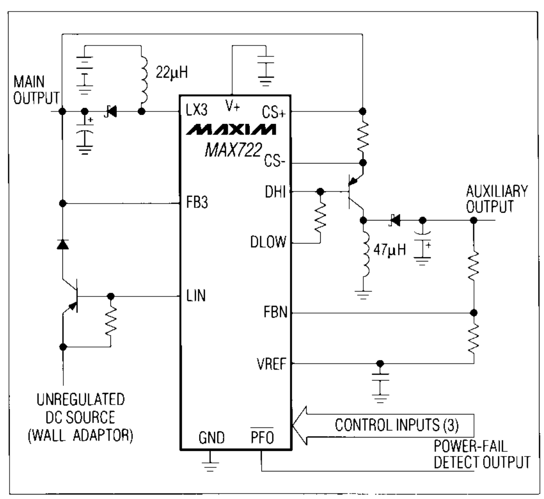
- ♦ **Low 0.9V to 5.5V Battery Input Range**
- ♦ **Unregulated 7V to 20V DC Input Range**
- ♦ **Dual Regulated Outputs**
  Main Output: 3.3V/5V
  Auxiliary Output: 0V to -100V
- ♦ **87% Efficiency at 200mA**
- ♦ **Efficient PRAM Keep-Alive: 80% at 1mA**
- ♦ **8W/in^3 Power Density**
- ♦ **60µA Quiescent Current**
- ♦ **20µA Shutdown Mode with VREF Alive**
- ♦ **500kHz Maximum Switching Frequency**
- ♦ **±1.5% VREF Tolerance (Over Temp.)**
- ♦ **Detect Output Power Failures**
- ♦ **16-Pin Narrow SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX722CSE	0°C to +70°C	larrow SO
MAX722C/D	0°C to +70°C	Dice*
MAX722ESE	-40°C to +85°C	16 Narrow SO
MAX723CSE	0°C to +70°C	16 Narrow SO
MAX723C/D	0°C to +70°C	Dice*
MAX723ESE	-40°C to +85°C	16 Narrow SO
MAX722EVKIT-SO	0°C to +70°C	Evaluation Kit-Surface Mount

Contact factory for dice specifications.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) .... +7V, -0.3V
Switch Voltage (LX3 to GND) .... +7V, -0.3V
Linear Regulator Voltage (LIN to GND) .... +20V, -0.3V
Auxiliary Pin Voltages
(NEGON, FB3, $3/\overline{5}$, $\overline{SHDN}$, FBN, DHI, DLOW, VREF,
PFO, CS+, CS- to GND) .... -0.3V to (V+ + 0.3V)
Ground Voltage Difference (AGND to GND) .... ±0.3V
Feedback Input Current (FBN) .... ±10mA
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Ranges:
MAX72_C__ .... 0°C to +70°C
MAX72_ESE .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +160°C
Lead Temperature (soldering, 10 sec) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Main Output Voltage – Main SMPS Mode	2V < VBATT1 < 3V, 0mA < I_{LOAD} < 200mA, DC SOURCE = 0V (Note 1)	$3/\overline{5}$ = 3V	MAX722	3.17	3.3	3.43	V
			MAX723	2.88	3.0	3.12	
		$3/\overline{5}$ = 0V		4.8	5.0	5.2	
Main Output Voltage – Linear-Regulator Mode	7V < DC SOURCE < 18V, 0mA < I_{LOAD} < 500mA	$3/\overline{5}$ = 3V	MAX722	3.17	3.3	3.43	V
			MAX723	2.88	3.0	3.12	
		$3/\overline{5}$ = 0V		4.8	5.0	5.2	
Auxiliary Output Voltage	2V < VBATT2 < 5V, VBATT1 = 2.5V, External Reference = 3V, R4 = 170k, R5 = 30k, 0mA < I_{LOAD} < 5mA			-18	-17	-16	V
FBN Input Offset Voltage	$3/\overline{5}$ = 0V or 3V				±2	±20	mV
FBN Input Bias Current	FBN forced to 0V				-5	±100	nA
Minimum Start-Up Supply Voltage (VBATT1)	I_{LOAD} = 0mA				0.85		V
Minimum Start-Up Supply Voltage (DCSOURCE)					7.3	7.6	V
Current-Sense Limit Threshold	Measured at CS+, CS-			170	200	230	mV
DHI Source Current	$3/\overline{5}$ = 3V				50		mA
DLOW On Resistance	$3/\overline{5}$ = 3V				5		Ω
Quiescent Supply Current from $3V_{OUT}$ (Note 2)	NEGON = 0V, $3/\overline{5}$ = 3V, FB3 forced to 3.47V (MAX722) FB3 forced to 3.15V (MAX723)					60	µA
Battery Quiescent Current (VBATT1 + VBATT2)	NEGON = 0V, $3/\overline{5}$ = 3V				60		µA
Shutdown Battery Current	NEGON = 0V, $3/\overline{5}$ = 3V, $\overline{SHDN}$ = 0V				20	40	µA
Battery Quiescent Current – Linear-Regulator Mode	DC SOURCE = 7V, $3/\overline{5}$ = 0V, measured at VBATT1			-10		10	µA
Linear-Regulator Output Sink Current	LIN = 6V, $3/\overline{5}$ = 3V, measured at LIN			20	50		mA
Reference Voltage	No VREF load			1.23	1.25	1.27	V
Reference Load Regulation	$3/\overline{5}$ = 3V, -20µA < REF load < 250µA		T_A = +25°C		10	20	mV
			T_A = T_{MIN} to T_{MAX}			25	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Fail Threshold	3/$\overline{5}$ = 0V or 3V, falling edge, referred to no-load output voltage	-4	-6	-8	%
Power-Fail Hysteresis	3/$\overline{5}$ = 0V or 3V		2		%
$\overline{PFO}$ Output Voltage Low	I_{SINK} = 2mA, 3/$\overline{5}$ = NEGON = 0V			0.4	V
$\overline{PFO}$ Output Current High	$\overline{PFO}$ = 4.8V, 3/$\overline{5}$ = 0V			1	µA
Logic Input Voltage Low	Measured at NEGON, $\overline{SHDN}$, 3/$\overline{5}$			0.4	V
Logic Input Voltage High	Measured at NEGON, $\overline{SHDN}$, 3/$\overline{5}$	1.6			V
Logic Input Current				±100	nA

Note 1: The main SMPS output voltage at full load current is guaranteed by measuring LX3 switch on resistance and peak current limit threshold.

Note 2: Supply current from $3V_{OUT}$ is measured with an ammeter between the main output $3V_{OUT}$ and FB3. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency.

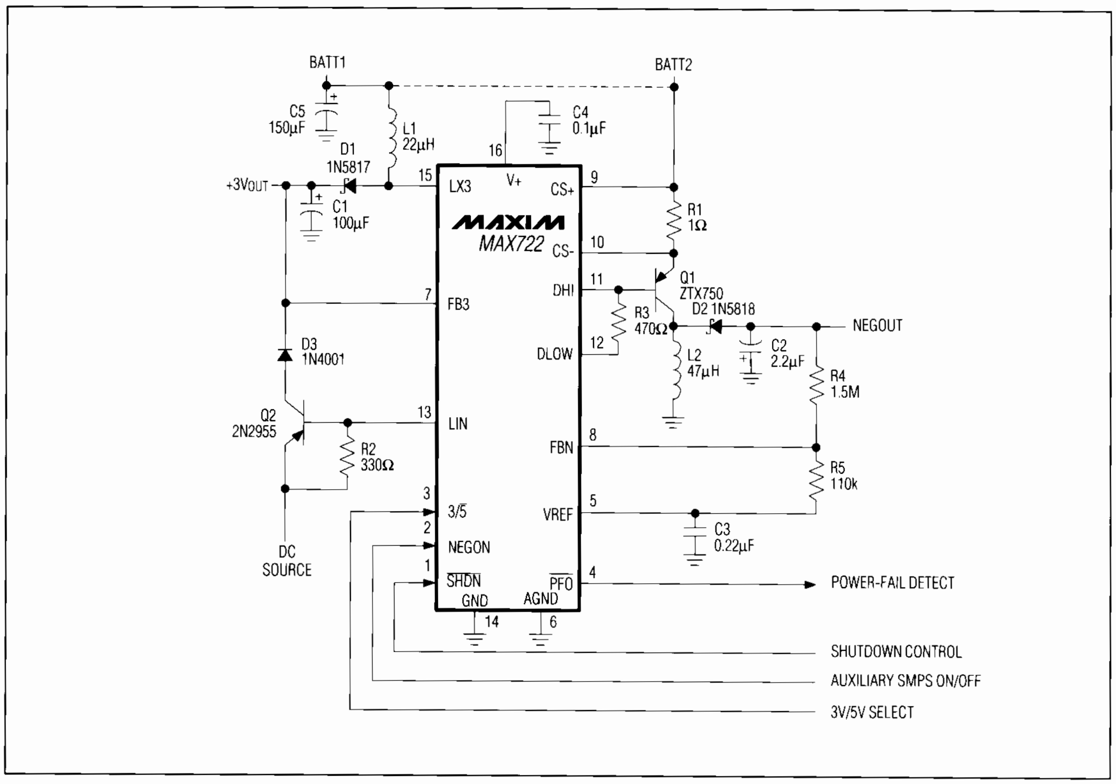
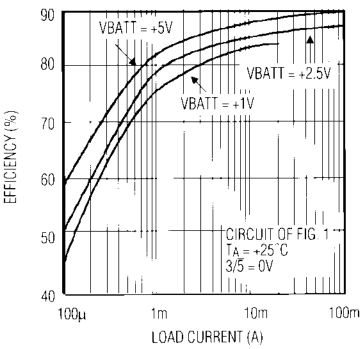


Figure 1. Standard Application Circuit

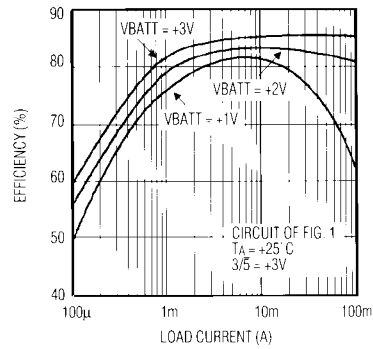
Palmtop Computer and LCD Power-Supply Regulators

Typical Operating Characteristics

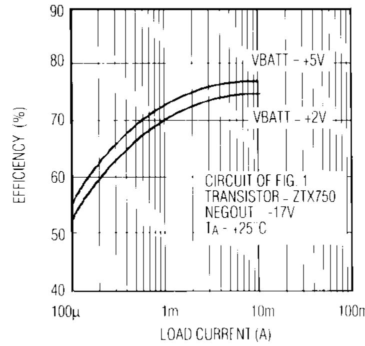
EFFICIENCY vs. LOAD CURRENT, MAIN SMPS IN 5V MODE



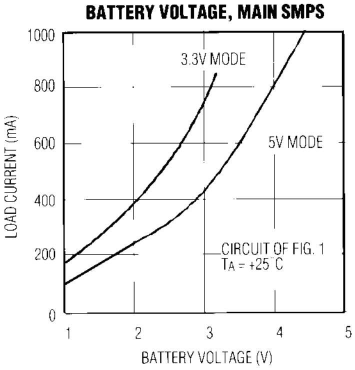
EFFICIENCY vs. LOAD CURRENT, MAIN SMPS IN 3.3V MODE



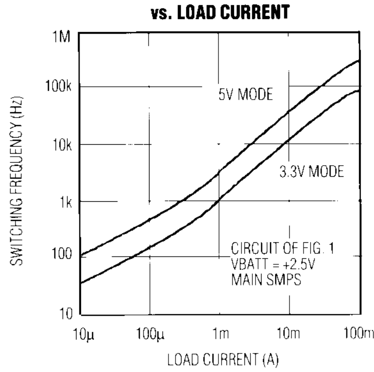
EFFICIENCY vs. LOAD CURRENT, AUXILIARY SMPS



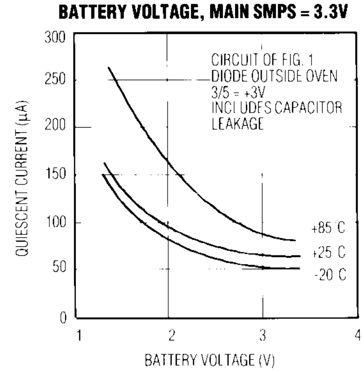
LOAD CURRENT CAPABILITY vs. BATTERY VOLTAGE, MAIN SMPS



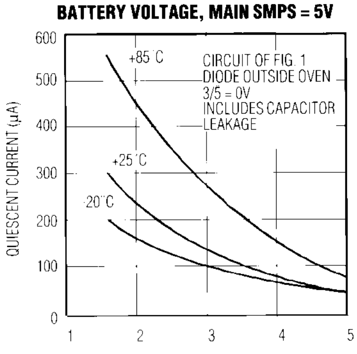
SWITCHING FREQUENCY vs. LOAD CURRENT



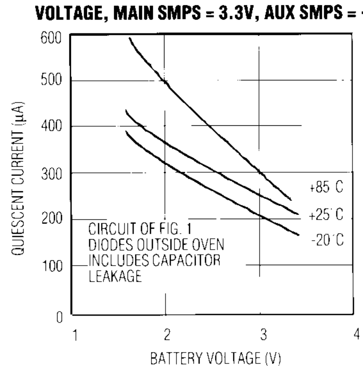
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 3.3V



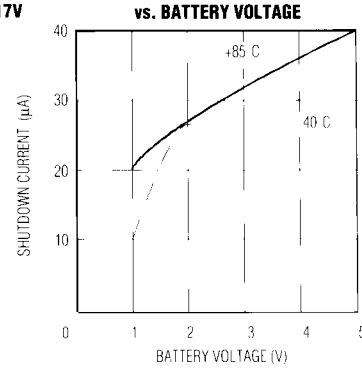
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 5V



BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 3.3V, AUX SMPS = -17V

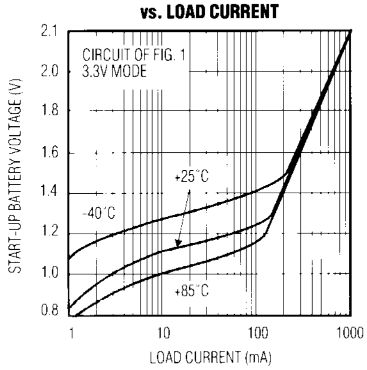


SHUTDOWN BATTERY CURRENT vs. BATTERY VOLTAGE

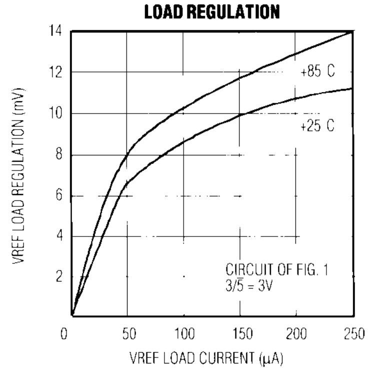


Typical Operating Characteristics (continued)

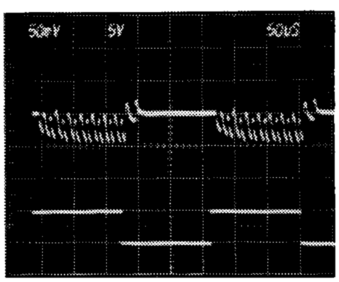
START-UP BATTERY VOLTAGE vs. LOAD CURRENT



REFERENCE VOLTAGE LOAD REGULATION



MAIN SMPS LOAD-TRANSTENT RESPONSE

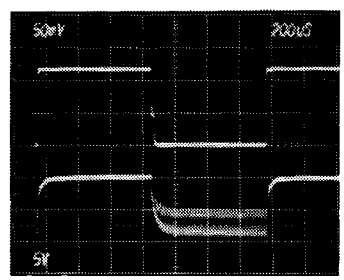


A = OUTPUT VOLTAGE, 50mV/div

B = LOAD CURRENT, 0mA TO 200mA

VBATT = 2.5V
HORIZONTAL = 50µs/div
3/5 = 0V

DC-SOURCE SWITCHOVER – SMPS TO LINEAR

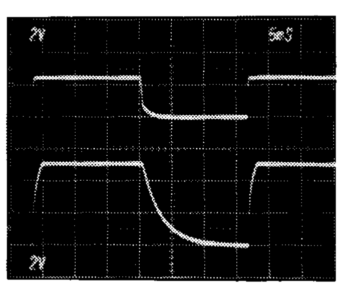


A = DC SOURCE, 0V to +12V

B = OUTPUT VOLTAGE, 50mV/div

I_{LOAD} = 200mA
HORIZONTAL = 200µs/div
3/5 = 0V

MAIN SMPS START-UP DELAY TIME



A = BATTERY VOLTAGE, 0V TO 2.5V

B = OUTPUT VOLTAGE, 2V/div

I_{LOAD} = 100mA
HORIZONTAL = 5ms/div
3/5 = 0V

Pin Description

PIN	NAME	FUNCTION
1	SHDN	Shutdown Input disables both SMPSs when low, but the reference remains alive. If the linear regulator is powered up, SHDN is overridden.
2	NEGON	Negative SMPS On/Off Control Input that enables the auxiliary negative SMPS when high.
3	3/5	Selects the main output voltage setting – 5V when low.
4	$\overline{PFO}$	Power-Fail Output - an open-drain output that goes low to indicate that the main output is out of regulation by 6% or more.
5	VREF	1.250V Reference Voltage Output. Bypass with 0.22µF capacitor to AGND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
6	AGND	Quiet Analog Ground
7	FB3	Feedback Input for the main SMPS
8	FBN	Feedback Input for the auxiliary negative SMPS
9	CS+	Positive Current-Sense Input for the auxiliary SMPS controller. 200mV corresponds with the maximum current limit threshold.
10	CS-	Negative Current-Sense Input
11	DHI	Driver for the auxiliary SMPS PNP. Open-drain P-channel output.
12	DLOW	Driver for the auxiliary SMPS PNP. Open-drain N-channel output. This output provides a controlled current sink to drive the PNP (set by an external limiting resistor).
13	LIN	Linear-Regulator Controller Output drives the external PNP pass transistor. Open-drain N-channel output. The main SMPS automatically shuts off when the voltage at LIN reaches 7.3V, and turns back on when LIN falls to 6.5V.
14	GND	Power Ground
15	LX3	1.2A, 0.4Ω N-channel power MOSFET drain for the main SMPS.

Detailed Description

Operating Principle

The MAX722/MAX723 combine two switch-mode power-supply (SMPS) regulators, a linear regulator, a precision voltage reference, and a power-fail detector (Figure 2). For maximum integration, the MAX722/MAX723 ICs contain internal N-channel power MOSFETs for the main low-voltage boost converter. This MOSFET is a "sense-FET" type for best efficiency, and has a very low gate-threshold voltage to guarantee start-up under low battery-voltage conditions (1.2V typ with 100mA load). The negative auxiliary controller exploits an external PNP transistor for the higher voltage requirement.

Pulse-Frequency Modulation

A unique minimum-off-time, current-limited, pulse-frequency modulation (PFM) control scheme is a key feature of both the main and auxiliary regulators (Figure 3). This PFM scheme combines the advantages of a pulse-width modulation scheme (PWM) (high output power and efficiency) with those of a traditional PFM pulse-skipper (ultra-low quiescent currents). There is no oscillator; switching is accomplished through a constant peak-current limit in the switch, which allows the inductor current to self-oscillate between this peak limit and some lesser value. Switching frequency is governed by a pair of one-shots that set a minimum off-time (1µs) and a maximum on-time (4µs). Under light loads, the inductor current rises to about one-half the current limit (for best light-load efficiency). Under heavy loads, the peak inductor current rises until it hits the current limit, whereupon the MOSFET switch turns off for the minumum off-time set by a one-shot. A switch to continuous-conduction mode results, which minimizes peak currents and component stresses for a given load. The only disadvantage of this architecture compared to full PWM operation is the variable-frequency switching noise. However, the noise does not exceed the current-limit times the filter capacitor equivalent series resistance (ESR), unlike conventional pulse-skippers.

Main 3V/5V Switch-Mode Regulator

The main output voltage can be selected to 3.3V or 5V with logic control, or it can be left in one mode or the other by tying 3/5 to ground or FB3. Efficiency varies depending on the battery and load, and is typically better than 80% over a 1mA to 200mA load range. The device is internally bootstrapped; power is derived from the output voltage (via FB3) or the battery (CS+ input), whichever is higher. When the output is set at 5V instead of 3.3V, the higher internal supply voltage results in lower switch transistor on-resistance and slightly greater output power. Bootstrapping allows the battery voltage to sag

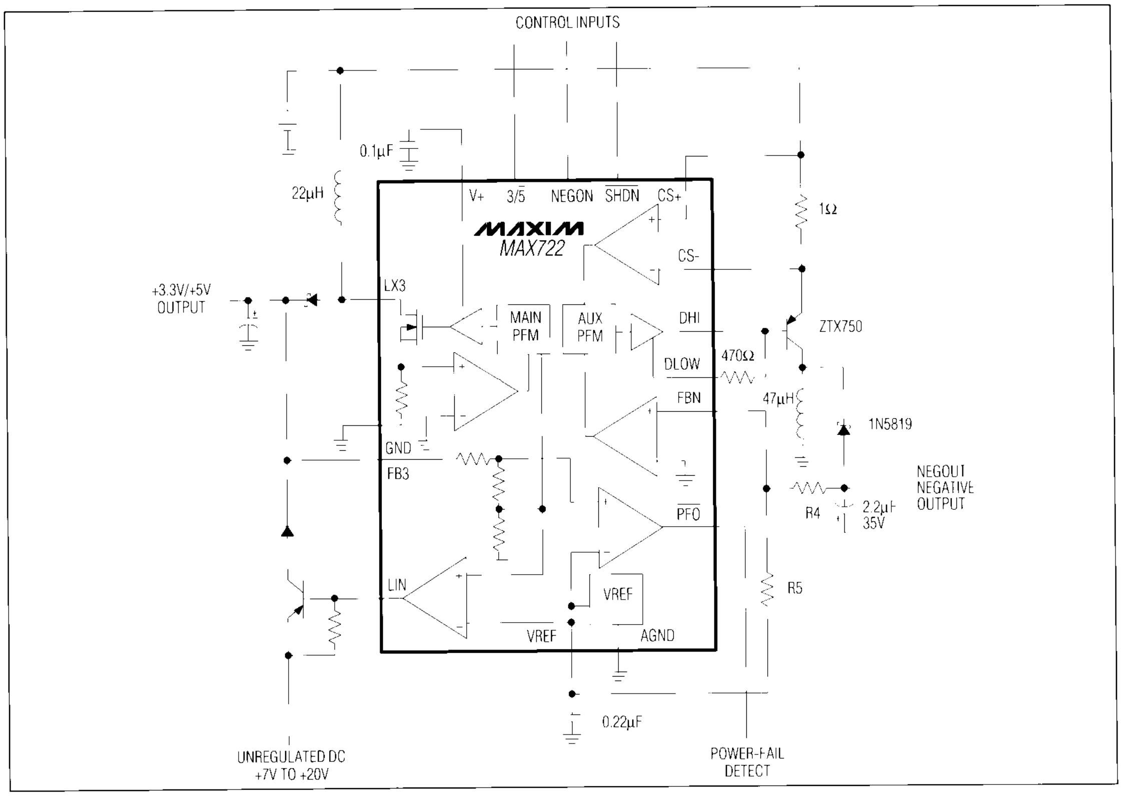


Figure 2. MAX722 Block Diagram

to less than 1V once the system is started. Therefore, the battery-voltage range is from V_{OUT} + V_{diode} to less than 1V (where V_{diode} is the forward drop of the Schottky rectifier). If the battery voltage exceeds the programmed output voltage, the output will follow the battery voltage. In many systems this is acceptable; however, the output voltage must not be forced above 7V.

The main regulator's peak current limit is internally fixed at 1A ±0.2A. The switching frequency depends on load and input voltage, and can range as high as 500kHz for the main SMPS.

Auxiliary Negative Switch-Mode Controller

The auxiliary controller operates similarly to the main regulator, except that the power transistor and sense resistor are external, and the maximum on-time is set at 8µs. Maximum possible output power is limited by the choice of external power transistor and sense resistor. A common 2N2907 works well as the switch transistor, but a high-gain fast PNP, such as the Zetex ZTX749 (preferred, but 25V BVCEO) or ZTX750 (40V BVCEO), provides typically 5% better efficiency.

The DHI and DLOW outputs provide a voltage source pull-up (DHI) and a current-sink pull-down (DLOW, set by the 470Ω resistor). This drive method is optimal for PNP transistors, so no external base speed-up capacitors are needed.

If the auxiliary regulator is always powered from a +5V source (such as the main output) or other relatively high-voltage input, a logic-level P-channel MOSFET in place of the PNP can provide typically > 80% efficiency (Figure 4).

The output voltage is set by R4 and R5 of Figure 1:

NEGOUT = -VREF(R4/R5)

NEGOUT can be made adjustable by making R4 a potentiometer, or by disconnecting VREF and driving R5 with a digital-to-analog converter or PWM signal.

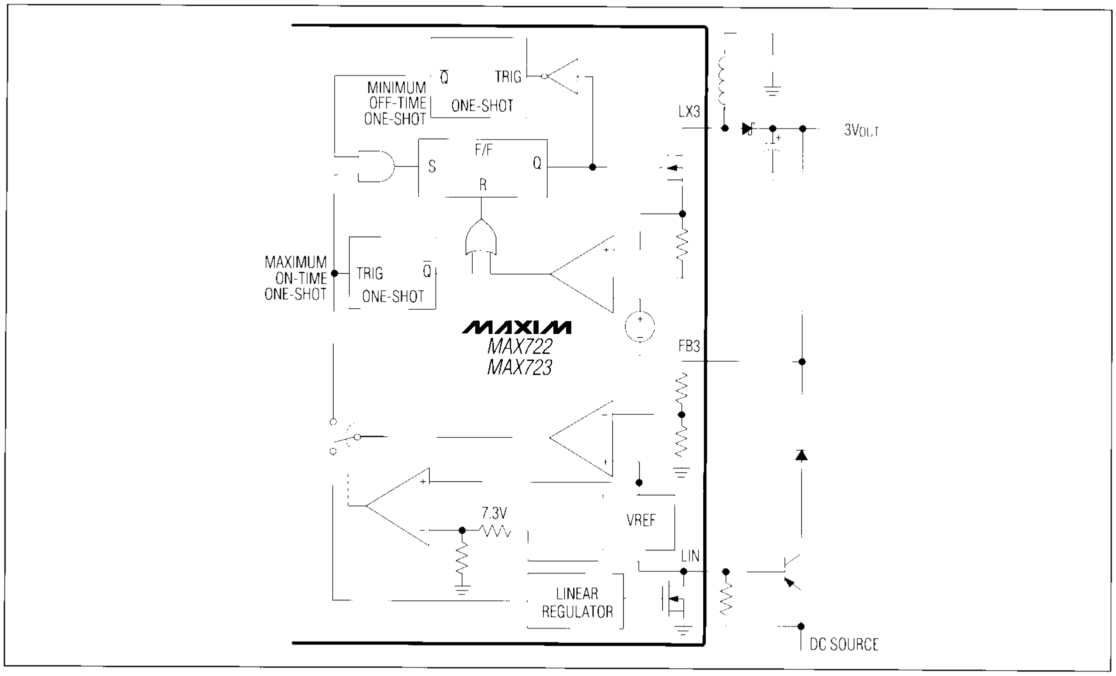


Figure 3. Main SMPS Block Diagram

The auxiliary SMPS peak current limit is set at 200mV/R1 (170mV worst-case low). The equations below calculate R1 based on design parameters. If the peak current limit is less than (NEGOUT) (1µsec/L), the circuit will operate in discontinuous-conduction mode. This is usually the case when low-voltage batteries and high LCD contrast voltages are employed. At low-output voltage settings, the circuit may enter continuous-conduction mode.

Discontinuous-conduction case:

$$I_{PEAK} = (2)(I_{LOAD})\left(1 + \frac{NEGOUT + VD}{VBATT - VSW}\right)$$

$$R1 = 200mV/I_{PEAK}$$

where VD is the forward voltage of the rectifier D2 and VSW is the average saturation voltage of the switch transistor Q1, including the drop across R1.

Discontinuous-mode example, -17V at 9mA from 2 AA batteries:

$$I_{PEAK} = (2)(9mA)\left(1 + \frac{17V + 0.5V}{2V - 0.3V}\right) = 203mA$$

$$R1 = 170mV/203mA = 0.83\Omega \text{ or less.}$$

Continuous-conduction case:

$$I_{PEAK} = (I_{LOAD})\left(\frac{NEGOUT + VD}{VBATT - VSW} + 1\right) + \left(\frac{NEGOUT + VD}{(2)(L)}\right)(1\mu s)$$

Continuous-mode example, -5V at 50mA from 3 AA batteries:

$$I_{PEAK} = 50mA\left(\frac{5V + 0.5V}{2.7V - 0.3V} + 1\right) + \left(\frac{5V + 0.5V}{(2)(47\mu H)}\right)(1\mu s) = 223mA$$

Powering the Auxiliary LCD Supply

The auxiliary output is not automatically powered from the linear regulator like the main output. The main battery will continue to drain if the auxiliary supply is not turned off when an external DC source is applied. There are several alternative solutions:

1. Power the LCD supply from the main output all the time. This leads to compounded efficiency losses, but is simple. These compounded losses are actually not crippling in many cases, especially if the main output is set

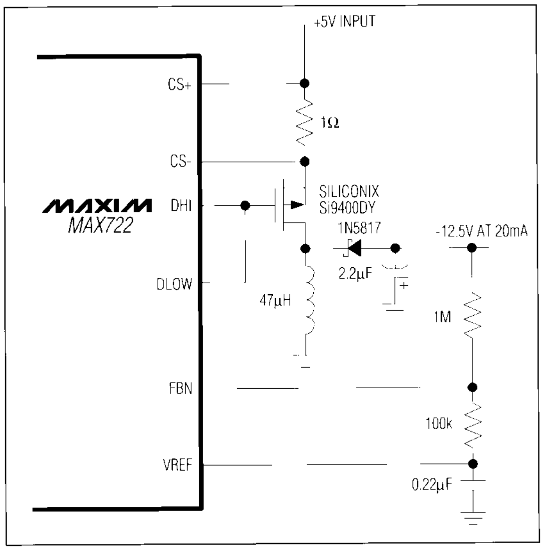


Figure 4. +5V-Powered LCD Supply with P-Channel MOSFET

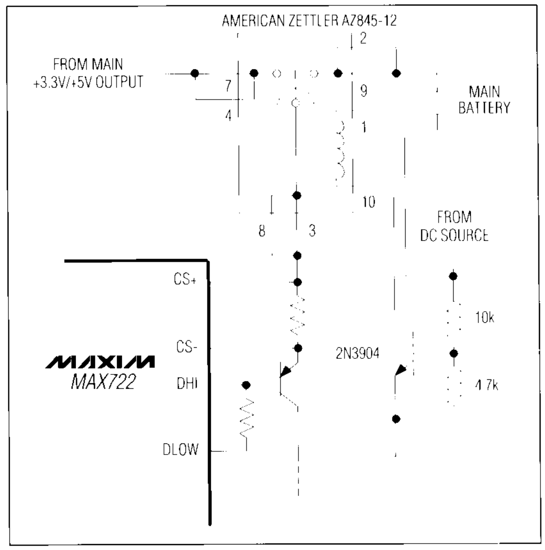


Figure 5. SMT Relay Powers Auxiliary LCD Supply

at 5V and the P-channel solution (Figure 4) is employed. For example, the overall efficiency for 2.5V to 5V at 50mA plus -17V at 5mA, when compounded by the P-channel circuit, is 81% vs. 84% for the non-compounded case (with PNP transistor).

2. Power the LCD supply from the main output in linear regulator mode, but power it from the battery when the DC source is absent. This provides the best overall efficiency, but requires a relay or MOSFET switch to make the switchover (Figure 5). In most applications, the battery voltage is too low to use P-channel devices for the switchover, but a high-side supply, such as the MAX623 charge-pump regulator (Figure 6) or the system +12V supply, works well with N-channel switches. Switchover can also be accomplished using special AC/DC adapter plugs and jacks with built-in mechanical switches.

3. Use a battery charger that can supply a load while it charges the battery, such as the MAX713. This approach also eliminates the PNP pass transistor for the linear regulator.

Linear Regulator

The linear regulator output drives the base of an external PNP pass transistor through an open-drain output. This design relies on a relatively slow PNP transistor for AC stability, so use a transistor with less than 10MHz f_t, or add a 1μF base-emitter capacitor. The base-emitter resistor should not be higher than 1kΩ unless a low-leakage PNP is used for the pass transistor.

When constructed with a 2N2955 PNP transistor, the typical output current capability is greater than 1A.

When the linear regulator operates, the main SMPS is disabled so as not to drain the battery. This mode cannot be programmed, but occurs automatically when LIN is pulled high by the external DC source.

Voltage Reference

The precision voltage reference is suitable for driving external loads such as a low-battery detection comparator or an analog-to-digital converter. It has guaranteed 250μA source- and 20μA sink-current capability. The reference is kept alive even in shutdown mode. If the reference drives an external load, bypass it with 0.22μF to ground. If the reference is unloaded, bypass it with a 0.1μF capacitor, minimum.

Power-Fail Status Output

The power-fail detector output (PFO) is an active-low, open-drain type. Although a true open-drain type, which can be wire-OR'ed with external logic, PFO is protected against ESD damage by reverse-biased clamp diodes connecting to V+. If $\overline{PFO}$ is pulled up to external supply voltages above the main output voltage level, the pull-up resistor must limit the current through the ESD protection diode to 25μA or less to maintain regulation of the outputs.

The $\overline{PFO}$ comparator senses when the main output is more than 6% out of regulation, and has 2% hysteresis

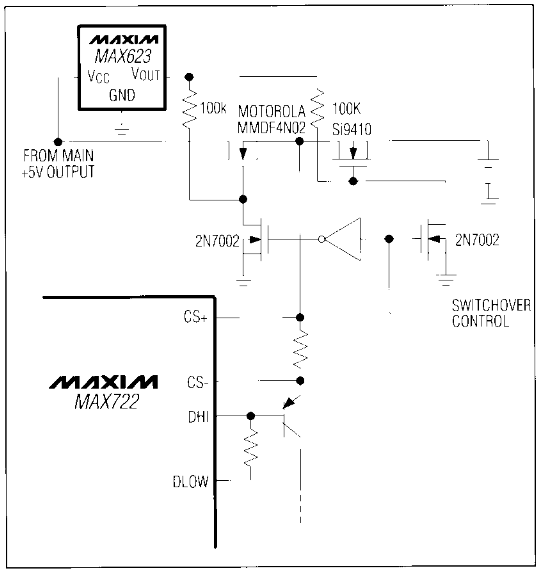


Figure 6. High-Side MOSFET Switch Powers Auxiliary LCD Supply

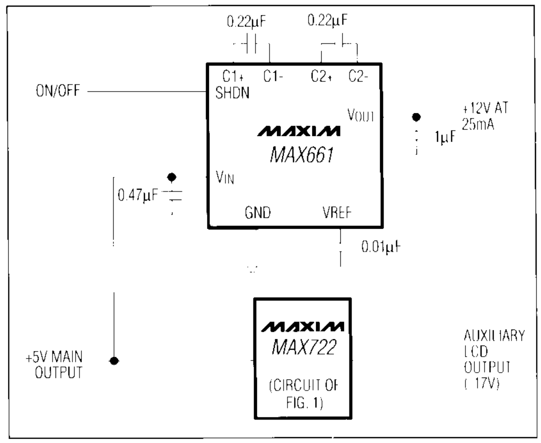


Figure 7. MAX722/MAX661 Triple-Output Supply with +12V for Flash Memory

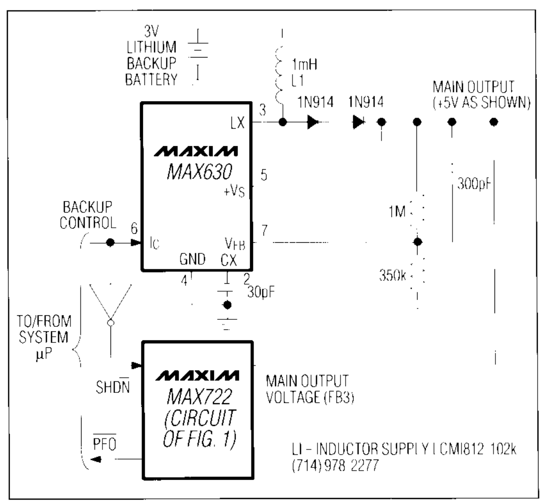


Figure 8. Lithium Backup-Battery Circuit

built in to prevent chatter. The $\overline{\text{PFO}}$ comparator is active in all modes except shutdown.

Control-Logic Inputs

The control inputs (3/$\overline{5}$, NEGON, and $\overline{\text{SHDN}}$) are high-impedance MOS gates protected against ESD damage by normally reverse-biased clamp diodes. If these inputs are driven from signal sources that exceed the main supply (FB3) voltage, the diode current should be limited to 25μA or less by a series resistor (1MΩ suggested). The logic input thresholds are the same (approximately 1V) in both 3V and 5V modes. Do not leave the control inputs floating.

Substrate Switchover Circuit

The substrate (V+, pin 16) is powered from either the battery (CS+ input) or from the main +3V output, whichever is higher. The substrate serves as the positive supply rail for most internal circuitry, including the reference and the PNP driver (DHI). Do not load V+. V+ must be bypassed to ground with at least 0.1μF.

Inductor Selection

The inductors must have a saturation (incremental) current rating equal to the peak switch current limit, which is 1.2A (worst-case) for the main output and user-adjustable for the auxiliary output. However, it's generally acceptable to bias the inductor deep into saturation by 20% or more.

The inductor's DC resistance significantly affects efficiency. For highest efficiency, limit L1's DCR to 0.03Ω or less.

Capacitor Selection

A 100μF, 10V SMT tantalum capacitor typically maintains 50mV$_{P-P}$ output ripple when stepping up 2V to 5V at 200mA. Smaller capacitors, down to 10μF, are acceptable for light loads or in applications that tolerate higher output ripple.

For the auxiliary output, a 2.2µF, 25V SMT tantalum capacitor typically provides 100mV$_{p-p}$ output ripple when inverting 3V to -17V at 5mA. Smaller capacitors down to 1µF are acceptable.

The ESR of both bypass and filter capacitors affects efficiency. Best performance is obtained by doubling up on the filter capacitors or using specialized low-ESR capacitors.

The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D series, which are about half the size of competing products. Sanyo OS-CON organic semiconductor through-hole capacitors also exhibit very low ESR.

Sprague: (603) 224-1961 or (207) 324-4140
Sanyo: (619) 661-6322

Applications Information

Lithium Backup-Battery Circuit

The MAX630 backup battery circuit of Figure 8 provides a low-current supply voltage of 3.3V or 5V to keep the system memory alive when the main battery pack is removed. When $\overline{PFO}$ goes low, the system must latch off the MAX722 and latch on the MAX630, periodically testing for the presence main battery's by going back to the original state after some interval. This method also extends the life of the expensive lithium battery by allowing a discharged main battery to "rest," allowing all of its energy to be used. The second rectifier diode allows this circuit to meet Underwriters Laboratories' requirements for preventing accidental charging of lithium batteries.

$\overline{PFO}$ remains active in shutdown mode.

PC Layout and Grounding

The MAX722's high peak currents and high-frequency operation make PC layout important for minimizing ground bounce and noise. Use the PC layout of Figures 9 and 10 as a rough guide for component placement and ground connections. The distance between the MAX722's GND and the ground leads of C1 and C5 must be kept to less than 0.2 inches (5mm). If possible, use a ground plane.

3-Cell Applications

Higher input voltages increase the energy transferred with each cycle, due to the reduced input/output differential. Excess ripple due to increased energy transfer is best minimized by reducing the inductor value (10µH suggested). Add extra filtering and recalculate the auxiliary regulator's current limit resistor value according to the equations under the *Auxiliary Negative Switch-Mode Controller* section.

Palmtop Computer and LCD Power-Supply Regulators

EV Kit General Description

The MAX722 evaluation kit (EV kit) is an assembled surface-mount demonstration board. The kit embodies the standard 2-cell application circuit of Figure 1, and adds a DIP switch and 3MΩ pull-up resistors for each control input. A MAX722 comes installed on the board, and it also accomodates a MAX723 footprint. To replace the MAX722 IC, first cut the leads free of the package, then carefully desolder the leads individually.

Operating Instructions

For best efficiency, connect heavy-gauge (18AWG) stranded wire from the battery terminals to a 2A adjustable supply or 2-cell battery pack.

Important: Connect BATT1 and BATT2 together with heavy wire to ensure both SMPS regulators work. If BATT1 is powered separately from BATT2, connect a new input bypass capacitor across BATT1 (not included). Otherwise, there is no filtering at BATT1 and efficiency will be poor.

Adjust the supply up to two or three volts. Load the outputs and observe the switching waveforms at LX3 and DHI.

EV Kit Component List

DESIGNATION	DESCRIPTION	SOURCE
C1	100µF, 10V E-size SMT tantalum capacitor	Matsuo 267M1002-107
C2	2.2µF, 35V C3-size SMT tantalum capacitor	Matsuo 267M2502-335
C3	0.22µF 1206-size ceramic capacitor	Murata-Erie GRM42-6X7R224K025V
C4	0.1µF 1206-size ceramic capacitor	Murata-Erie GRM42-6X7R104K025V
C5	150µF, 6.3V E-size SMT tantalum capacitor	Matsuo 267M6301-157
C6	Not used	
L1	22µH, 1A SMT inductor	Sumida CD54-220 or two CD43-220 in parallel
L2	47µH, 0.25A SMT inductor	Sumida CD54-470
R1	1Ω ±10% 1206-size chip resistor	Ohmtek L1206MR1R00LB
R2	330Ω ±5% 1206-size chip resistor	
R3	470Ω ±5% 1206-size chip resistor	
R4	1.5MΩ ±1% 1206-size chip resistor	
R5	110kΩ ±1% 1206-size chip resistor	
D1	1A SMT Schottky rectifier, 1N5817 equivalent	NIEC EC15QS02L
D2	1A SMT Schottky rectifier, 1N5818 equivalent	NIEC EC10QS03
D3	1A SMT silicon rectifiers, 1N4001 equivalent	NIEC EC10DS1
Q1	Fast, high-gain, low sat 30V PNP transistor	Zetex ZTX750SM
Q2	Power PNP transistor, D-PAK	Motorola MJD2955

Matsuo USA	(714) 969-2491 FAX (714) 960-6492
Matsuo Japan	(06) 332-0871
Motorola	(602) 244-6900
Murata-Erie	(404) 436-1300
NIEC	(805) 867-2555
NIEC Japan	(81) 3-3494-7411
Ohmtek	(716) 283-4025
Siliconix	408) 988-8000
Sumida USA	(708) 956-0666
Sumida Japan	(03) 3607-5111 FAX (03) 3607-5428
Zetex	(516) 543-7100

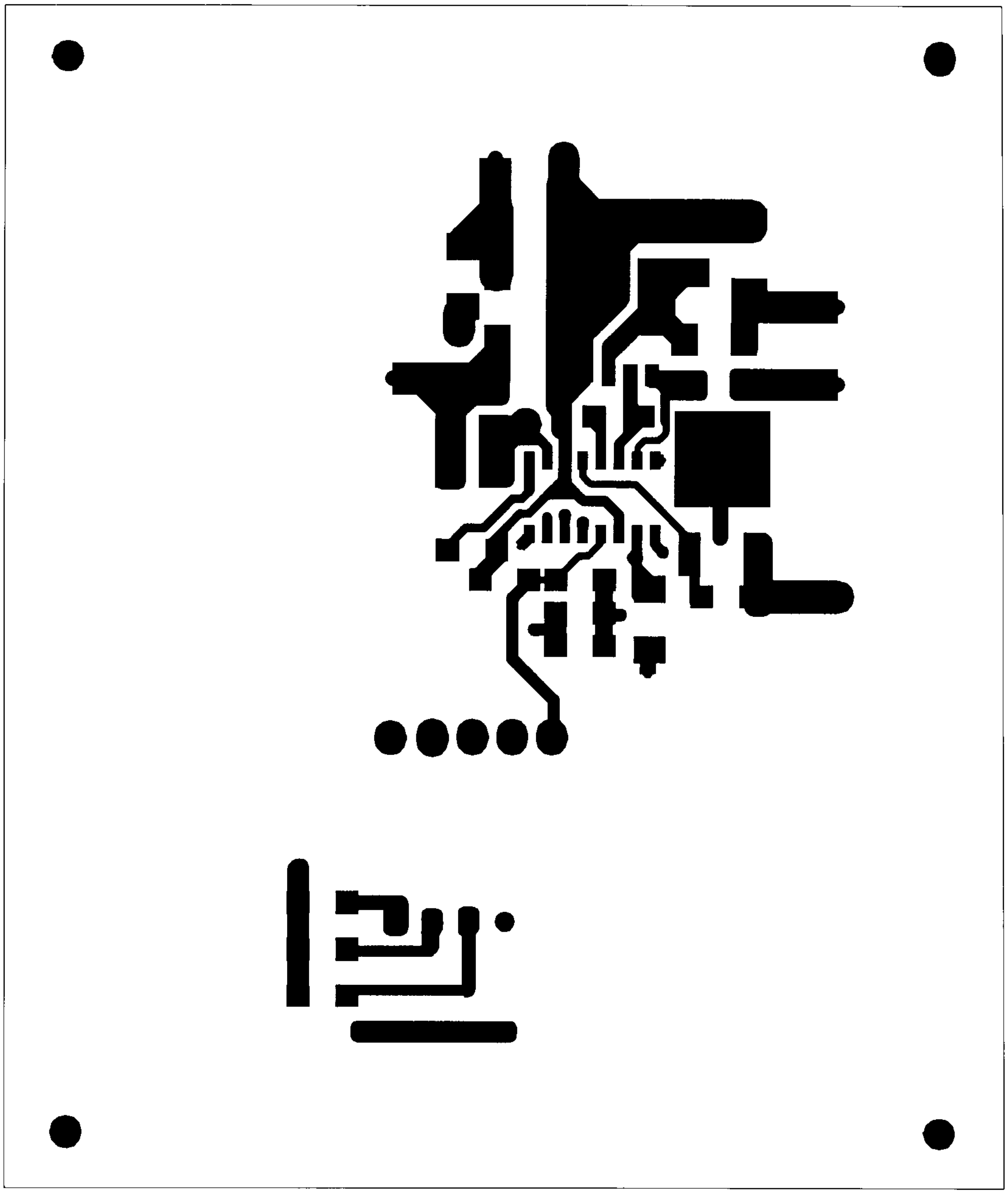


Figure 9. MAX722 EV Kit PC Layout (Component Layer, Component Side View, 2X Scale)

Palmtop Computer and LCD Power-Supply Regulators

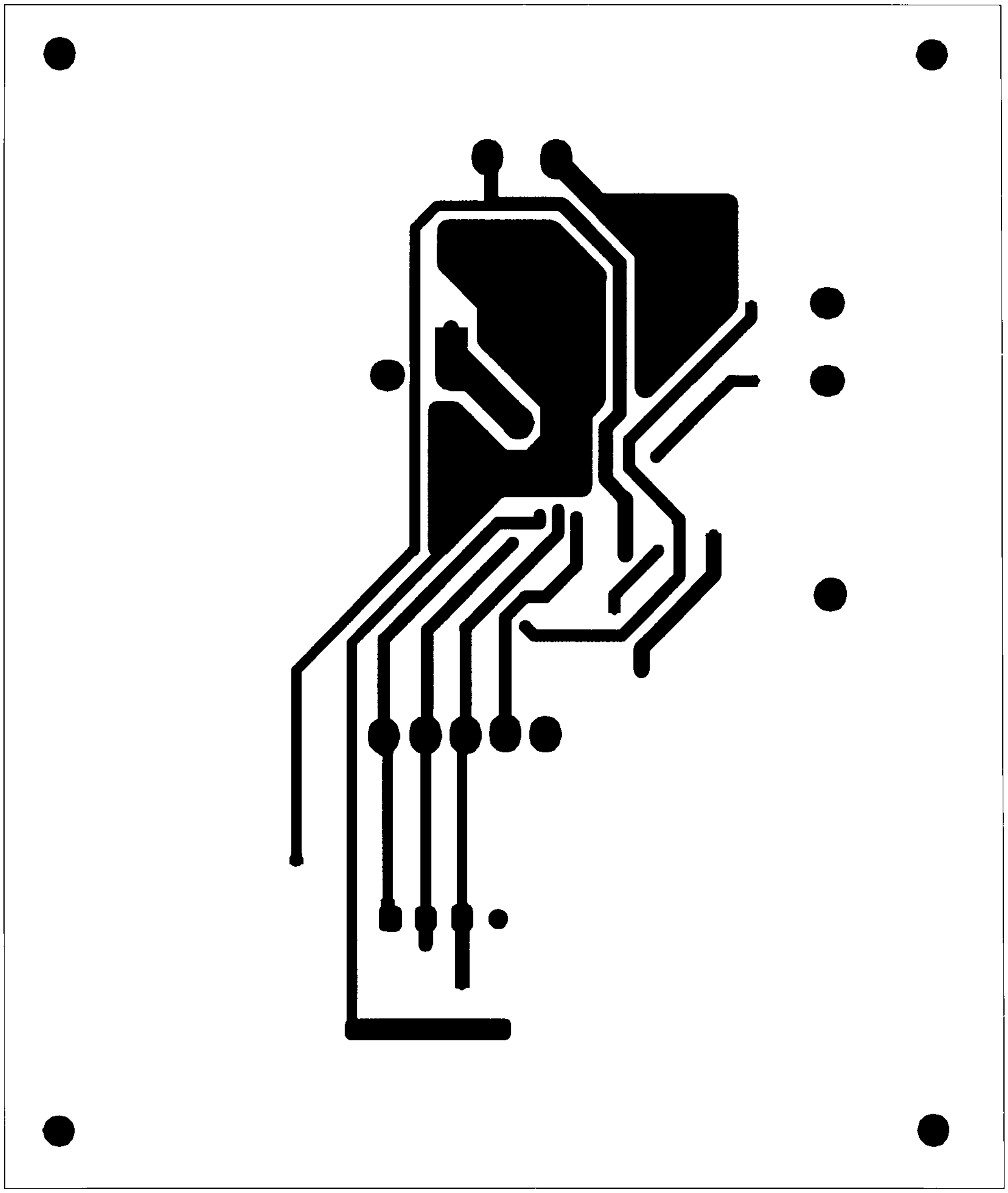


Figure 10. MAX722 EV Kit PC Layout (Bottom Layer, Component Side View, 2X Scale)

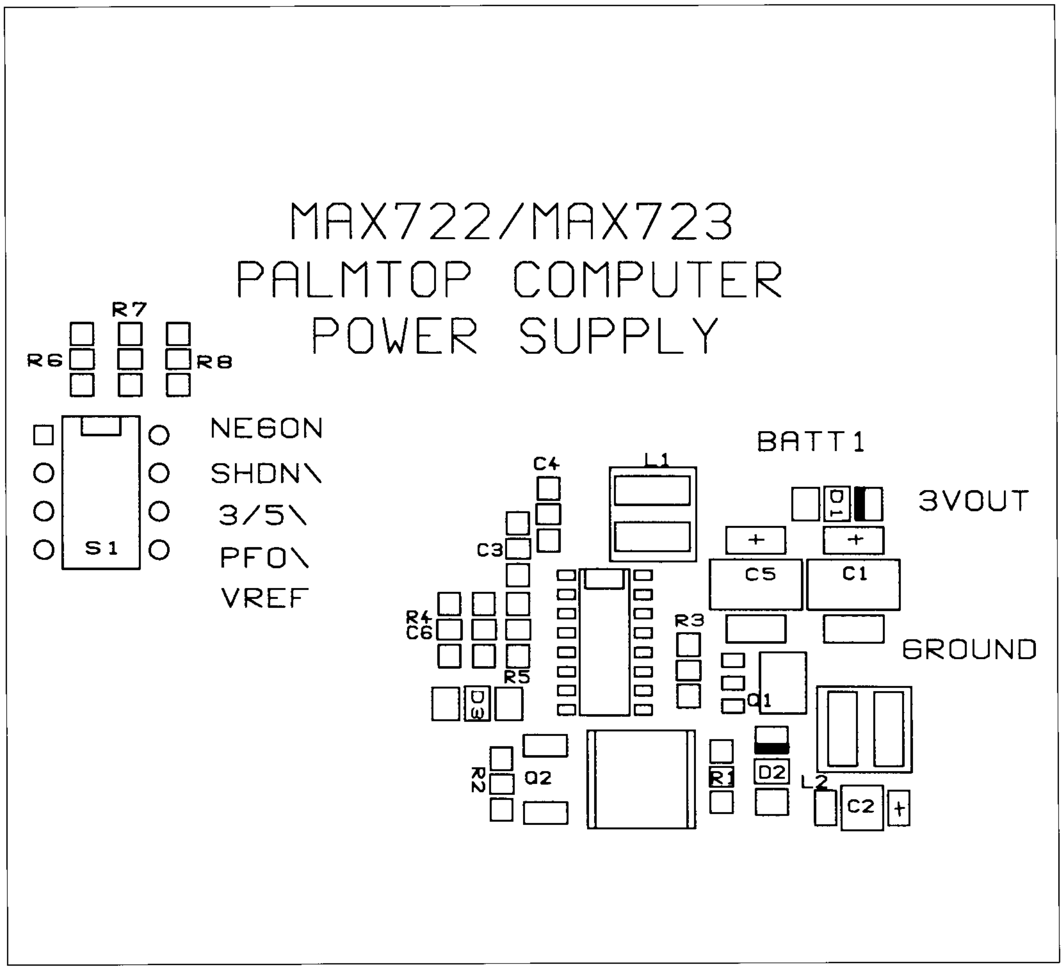
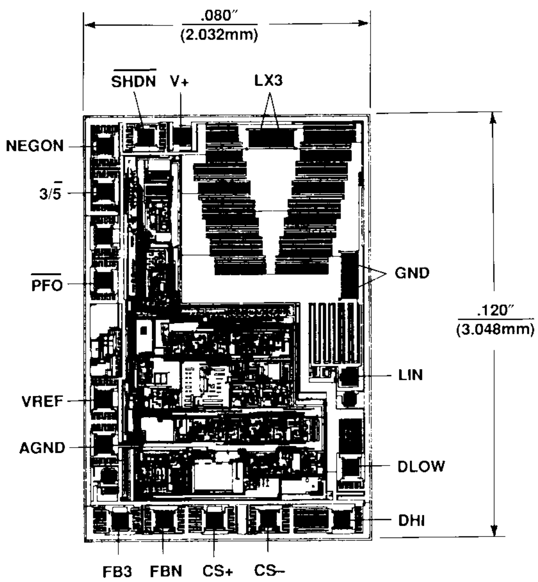


Figure 11. MAX722 EV Kit Component Placement Diagram

Palmtop Computer and LCD Power-Supply Regulators

Chip Topography



TRANSISTOR COUNT: 743.
SUBSTRATE IS CONNECTED TO V+.