Cyclone V GT FPGA Development Kit

User Guide

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

1. About This Kit

This chapter introduces the major components of The Altera® Cyclone® V GT FPGA Development Kit. This kit is a complete design environment that includes both the hardware and software you need to develop and prototype Cyclone V GT FPGA designs.

Kit Features

This section briefly describes the Cyclone V GT FPGA Development Kit contents.

Hardware

The Cyclone V GT FPGA Development Kit includes the following hardware:

- Cyclone V GT FPGA development board
- Debug Header Breakout Board HSMC
- Loopback Daughtercard HSMC
- Power supply and cables:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - Mini SMB cable

For a complete list of this kit's contents and capabilities, refer to the Cyclone V GT FPGA Development Kit page.

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

Cyclone V GT FPGA Development Kit Installer

The license-free Cyclone V GT FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Installing the Development Kit" on page 3–2.

2. Getting Started

This chapter provides the initial guidelines to get you started using the kit.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspecting the Boards

To inspect each board, do the following:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that components on the boards appear to be in place and intact.

In typical applications with the Cyclone V GT FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron CHR-152. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to "The Power Monitor" on page 6–17.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References for Getting Started

Use the following links to check the Altera website for other related information:

- For complete information about the FPGA development board hardware, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.
- For the latest board design files and reference designs, refer to the Cyclone V GT FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Cyclone V GT device documentation, refer to the Documentation: Cyclone V Devices page.
- To purchase devices from the eStore, refer to the Devices page.

- For Cyclone V GT OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition software
- Cyclone V GT FPGA Development Kit software
- On-Board USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

Included in the Quartus II Subscription Edition software are the Quartus II software (including Qsys), the Nios II EDS, and the MegaCore IP Library. To install the Altera development tools, do the following:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus II software installation directory.

If you have difficulty installing the Quartus II software, refer to the *Altera Software Installation and Licensing Manual*.

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the myAltera Account Sign In web page, and click **Sign In**.
2. On the myAltera Home web page, click the *Self-Service Licensing Center* link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code.

   The number consists of alphanumeric characters and does not contain hyphens: for example, *5xxxSoCxxxxxxx*.

4. On the Self-Service Licensing Center web page, click the *Find it with your License Activation Code* link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

For complete licensing details, refer to the *Altera Software Installation and Licensing Manual*.

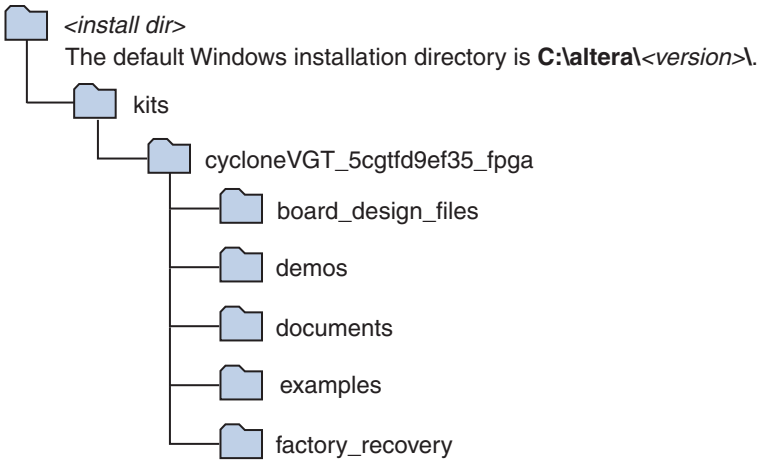
Installing the Development Kit

To install the development kit, do the following:

1. Download the Cyclone V GT FPGA Development Kit installer from the Cyclone V GT FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Start the Cyclone V GT FPGA Development Kit installer for Windows, or unzip the installation image for Linux.
3. Choosing an installation directory that is relative to the Quartus II software installation directory, follow the on-screen instructions to complete the installation process.

The installation program creates the Cyclone V GT FPGA Development Kit directory structure shown in Figure 3–1.

Figure 3–1. Cyclone V GT FPGA Development Kit Installed Directory Structure *(1)*



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Cyclone V GT FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Cyclone V GT FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

For installation instructions for the On-Board USB-Blaster II driver, refer to the Cable and Adapter Drivers Information page of the Altera website.

4. Development Board Setup

This chapter explains how to set up the Cyclone V GT FPGA development board and restore default settings.

Setting Up the Board

To configure and apply power to the board, do the following:

1. The FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch and Jumper Settings" on page 4–2 before proceeding.
2. The FPGA development board ships with design examples stored in flash memory. Verify the SW4.3 DIP switch is set to the FACT ON (logic 0) position to load the design stored in the factory portion of flash memory.

The FPGA development board can be powered by the PCIe host adapter or the laptop power adapter. If you want to power the board by the PCIe host system, plug the FPGA development card into a standard PCIe connector. Alternatively, to power the FPGA development board using the laptop power adaptor, do the following two steps:

3. Connect the +19 V (6.32 A) power supply to the DC Power Jack (J8) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

4. Set the POWER switch (SW2) to the ON position. When power is supplied to the board, blue LED (D21) illuminates indicating that the board has power.

The MAX V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The SW4.3 DIP switch controls which design to load. When the switch is in the FACT ON (logic 0) position, the PFL loads the design from the factory portion of flash memory.

The MAX V design resides in the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\examples\max5** directory.

When configuration is complete, the Config Done LED (D7) illuminates, signaling that the Cyclone V GT device configured successfully.

For more information about the PFL megafunction, refer to the *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch and Jumper Settings

Figure 4–1 shows the default switch settings for the top side of the Cyclone V GT FPGA development board.

Figure 4–1. Default Switch Settings on the Board Top

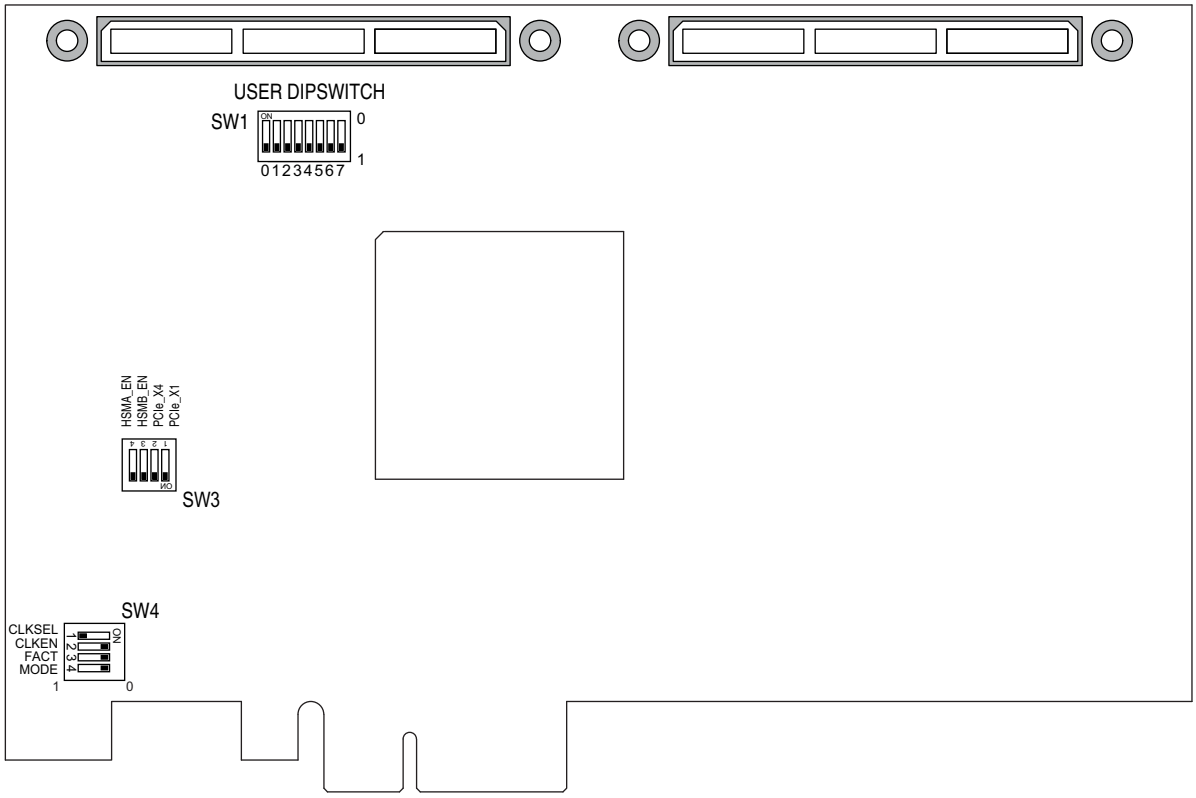
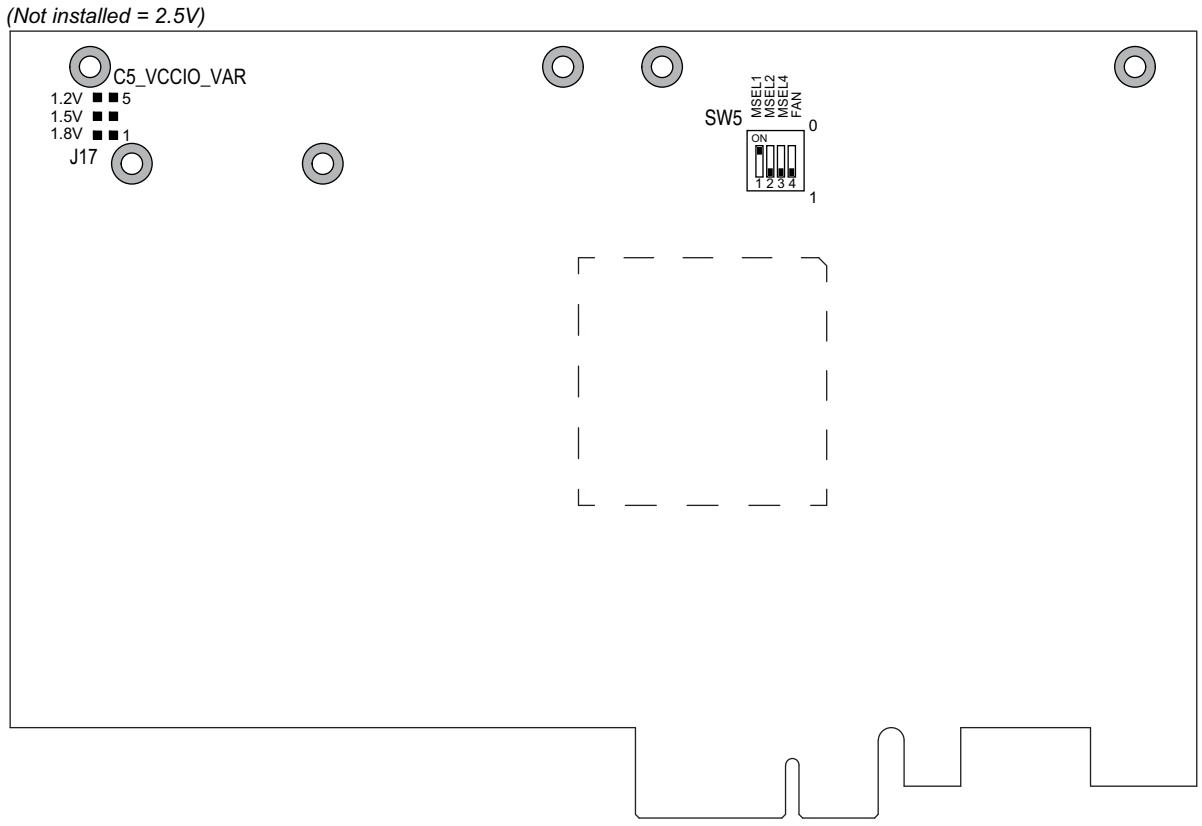


Figure 4–2 shows the default switch and jumper settings for the bottom side of the Cyclone V GT FPGA development board.

Figure 4–2. Default Switch Settings on the Board Bottom



The following tables do not describe user DIP switches.

To restore the switches to the default settings, do the following:

1. Set the DIP switch bank (SW3) to match Table 4–1 and Figure 4–1.

Table 4–1. SW3 DIP Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	PCIe_X1	Switch 1 has the following options: ■ ON (logical 0) = x1 presence detect is enabled. ■ OFF (logical 1) = x1 presence detect is disabled.	ON
2	PCIe_X4	Switch 2 has the following options: ■ ON (logical 0) = x4 presence detect is enabled. ■ OFF (logical 1) = x4 presence detect is disabled.	ON

Table 4–1. SW3 DIP Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	HSMB_EN	Switch 3 has the following options: ■ ON (logical 0) = HCMC Port B not in JTAG chain. ■ OFF (logical 1) = Include HCMC Port B in the JTAG chain.	ON
4	HSMA_EN	Switch 4 has the following options: ■ ON (logical 0) = HCMC Port A not in JTAG chain. ■ OFF (logical 1) = Include HCMC Port A in the JTAG chain.	ON

2. Set the DIP switch bank (SW4) to match Table 4–2 and Figure 4–1.

Table 4–2. SW4 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	CLKSEL	Switch 1 has the following options: ■ ON (logical 0) = SMA input clock select. ■ OFF (logical 1) = Programmable oscillator clock select.	OFF
2	CLKEN	—	ON
3	FACT	Switch 3 has the following options: ■ ON (logical 0) = Load the factory design from flash at power up. ■ OFF (logical 1) = Load the user design from flash at power up.	ON
4	MODE	Switch 4 is an optional user switch setting. It is not currently defined in the MAX 5 system controller.	ON

3. Set the DIP switch bank (SW5) to match Table 4–3 and Figure 4–2.

Table 4–3. SW5 DIP Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	MSEL1	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	ON
2	MSEL2	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Table 4–3. SW5 DIP Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	MSEL4	Switch 3 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
4	FAN	Switch 4 has is an optional user switch setting. It is not currently defined in the MAX 5 system controller.	OFF

For more information on the MSEL modes, refer to Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices.

4. Set the J17 jumper block to match Table 4–4 and Figure 4–2. The C5_VCCIO_VAR power rail provides the voltage to bank 7, which connects to the HSMB interface. By default this rail is 2.5 V. If needed, you can change the voltage level of this power supply by adding in a jumper wire between the pins of J17 as indicated in Table 4–4 and Figure 4–2.

Table 4–4. J17 Jumper Block *(1)*

Jumper	C5_VCCIO_VAR	Default Position
Pins 1-2	1.8 V	Not installed
Pins 3-4	1.5 V	Not installed
Pins 5-6	1.2 V	Not installed

Note to Table 4–4:

(1) Adding a single jumper between the pins sets the voltage as described in the table. Install only one jumper location at a time.

For more information about the FPGA board settings, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.

Configuring the MAX V Device to Program EPCQ

It is possible to configure the FPGA from the EPCQ device. However, the MAX V design provided with the Cyclone V GT FPGA development kit does not allow you to store a design in the EPCQ configuration device.

To enable FPGA configuration using the EPCQ device, reconfigure the MAX V device with the design file found at How do I access the EPCQ configuration device on the Cyclone V GT FPGA Development Kit?.

Restoring the MAX V CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX V CPLD on the FPGA development board. Make sure you have the Nios II EDS installed, and do the following:

1. Set the board switches to the factory default settings described in "Factory Default Switch and Jumper Settings" on page 4–2.
2. Start the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** for the 5M2210 MAX V device and select <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery\max5.pof**.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Cyclone V GT FPGA Development Kit page of the Altera website.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the FPGA development board. Make sure you have the Nios II EDS installed, and do the following:

1. Set the board switches to the factory default settings described in "Factory Default Switch and Jumper Settings" on page 4–2.
2. Start the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 4–7 for more information.
3. Click **Add File** and select <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery\c5gt_fpga_bup.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating that the flash device is ready for programming.
6. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
7. In the Nios II command shell, navigate to the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery** directory and type the following command to run the restore script:

   ```
   ./restore.sh ↵
   ```

   Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.
8. After all flash programming completes, if powered by the laptop power adapter, cycle the POWER switch (SW2) off then on. If the FPGA development board is powered by PCIe host, cycle the host power.
9. Using the Quartus II Programmer, click **Add File** and select <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery\c5gt_fpga_bup.sof**.
10. Turn on the **Program/Configure** option for the added file.

11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating the flash memory device is now restored with the factory contents.
12. After all flash programming completes, if powered by the laptop power adapter, cycle the POWER switch (SW2) off then on. If the FPGA development board is powered by PCIe host, cycle the host power.
13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

    ```
    nios2-terminal ↵
    ```

14. Follow the instructions in the terminal window to generate a unique MAC address.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Cyclone V GT FPGA Development Kit page of the Altera website.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific SRAM Object File (**.sof)**. Before configuring the FPGA, verify the following conditions:

- Quartus II Programmer and the USB-Blaster II driver are installed on the host computer.
- USB cable is connected to the FPGA development board.
- Power to the board is on.
- No other applications that use the JTAG chain are running.

To configure the Cyclone V GT FPGA, do the following:

1. Start the Quartus II Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications to lose their connection to the board. Restart those applications after configuration is complete.

If the Quartus II programming window is already open and you power cycle the board, to detect the JTAG chain, do the following:

- Click **Hardware Setup** in the Quartus II Programmer window.
- Reselect **USB-Blaster II**.

5. Board Update Portal

This chapter explains how you can connect to the Board Update Portal and use it to upload your own designs.

The Cyclone V GT FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the SW4.3 DIP switch in the FACT ON (logic 0) position, the FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides useful kit-specific links and design resources.

☞ After successfully updating the user hardware 1 flash memory, you can load a design from flash memory into the FPGA. To do so, set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

The source code for the Board Update Portal design resides in the *<install dir>***\kits\cycloneVGT_5cgtfd9ef35_fpga\examples** directory.

Connecting to the Board Update Portal Web Page

Ensure that you have the following items setup and installed:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, do the following:

1. With the board powered down, set the SW4.3 DIP switch to the FACT ON (logic 0) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
4. Start a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   ☞ You can click *Cyclone V GT FPGA Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Cyclone V GT FPGA Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Write User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format. However, if you have generated a SRAM Object File (**.sof)** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Design files available from the Cyclone V GT FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, do the following:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" on page 5–1 to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field. Otherwise, leave the **Software File Name** field blank.
3. Click **Upload** and then wait for the files to write to flash memory. A progress bar indicates the percent complete.
4. To configure the FPGA with the new design, set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page 4–6.

6. Board Test System

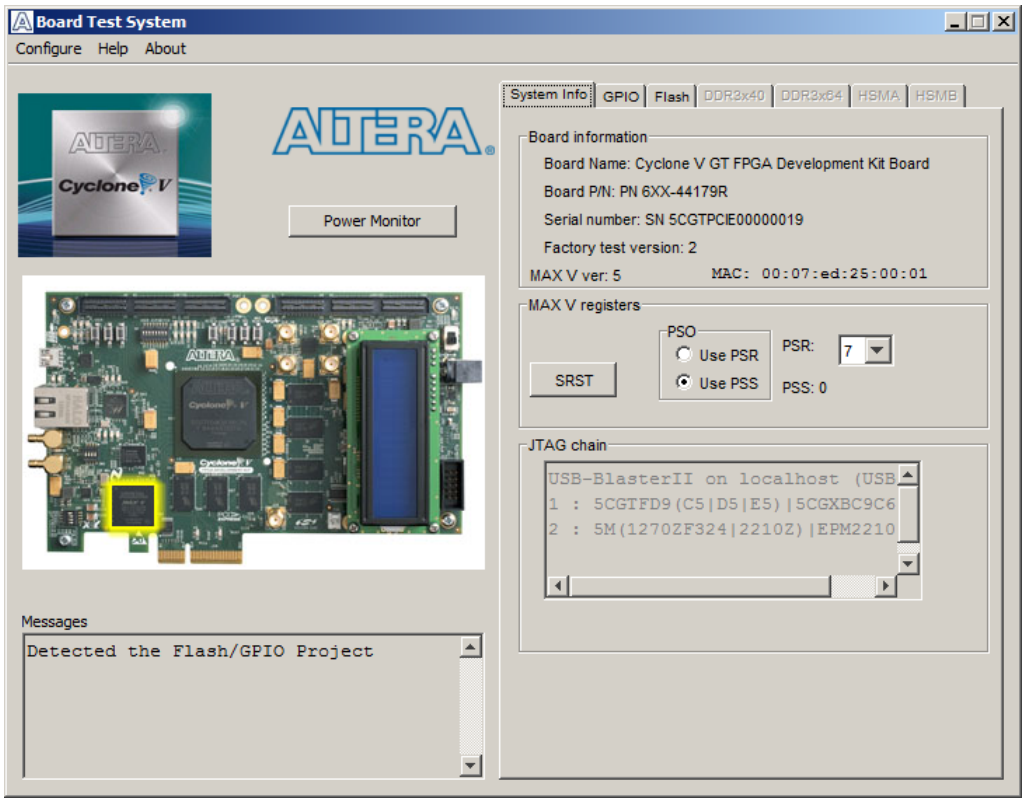
This chapter explains how you can use the Board Test System GUI to test board components, modify functional parameters, observe performance, and measure power usage.

Along with the Board Test System, the development kit includes related design examples. These designs are provided to test the major board features. Each design provides data for one or more tabs in the application. While using the Board Test System, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

The Board Test System is also useful as a reference for designing systems.

Figure 6–1 shows the GUI and initial **System Info** tab for a board in the factory configuration.

Figure 6–1. Board Test System GUI



Highlights appear in the board picture around the corresponding components.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing to Run the Board Test System

With the power to the board off, do the following:

1. Connect the USB cable to the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ45 connector.
3. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch and Jumper Settings" section starting on page 4–2.
4. Set the SW4.3 DIP switch to the FACT OFF (logic 1) position.
5. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. The design loads the **System Info**, **GPIO**, **Flash** tabs and related tests under the following conditions:
   - Your board is still in the factory configuration.
   - You have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal.

CAUTION

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the Board Test System, make sure you have first installed the software. Follow the steps in "Installing the Development Kit" on page 3–2.

You can start the Board Test System with the following:

- The **BoardTestSystem.exe** application that resides in <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\examples\board_test_system** directory.
- The Windows Start menu: **All Programs > Altera > Cyclone V GT FPGA Development Kit** <*version*> **> Board Test System**.

Once the Board Test System application GUI appears, it displays the application tab that corresponds to the design running in the FPGA. The board's flash memory ships preconfigured with the design that corresponds to the **System Info**, **GPIO**, **Flash** tabs.

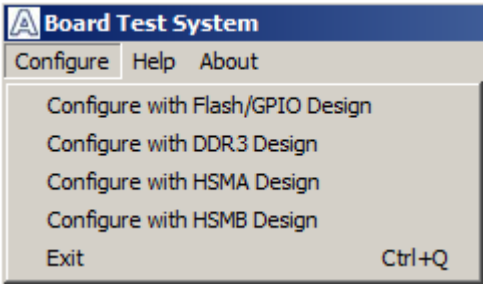
Using the Board Test System

This section describes the menus and controls on the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 6–2) to select the design you want to use. Each design example on this menu tests different board features that corresponds to one or more application tabs. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, do the following:

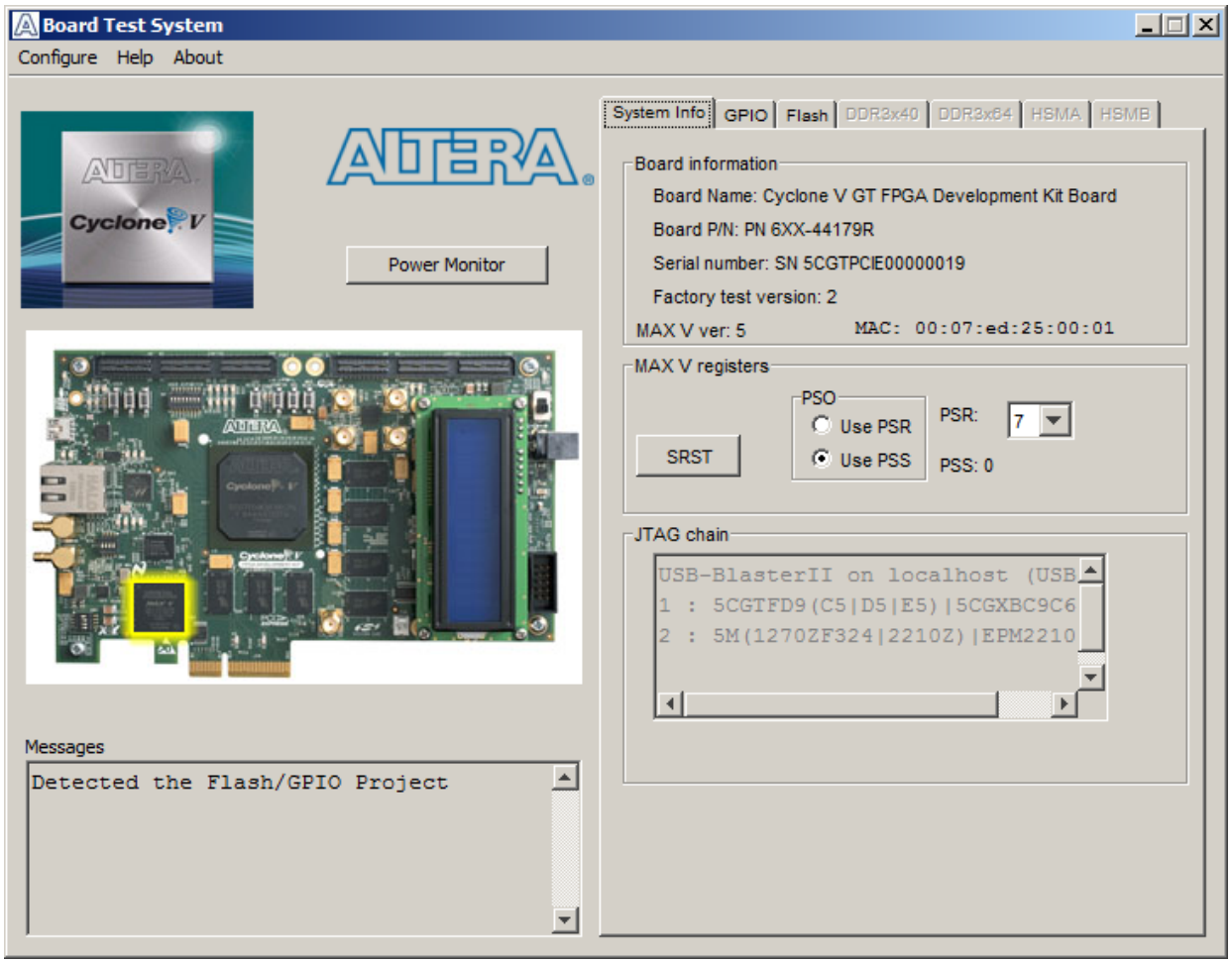
1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. When configuration finishes, close the Quartus II Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

☞ If the Board Test System application is open while you configure FPGAs with the Quartus II Programmer, you may need to restart the Board Test System.

The System Info Tab

The **System Info** tab displays the board's current configuration and allows you to change MAX V register values. Figure 6–3 shows the **System Info** tab with the MAX V highlighted in the photograph.

Figure 6–3. The System Info Tab



The following sections describe the controls on the **System Info** tab.

Power Monitor

Clicking this control starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX V device, you can measure the power of any design in the FPGA, including your own designs. For more information, refer to "The Power Monitor" on page 6–17.

Board Information

This group control displays static information about your board:

- **Board Name**—Indicates the official name of the board.

- **Board P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAX V ver**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\examples** directory.

  Newer revisions of this code might be available on the Cyclone V GT FPGA Development Kit page of the Altera website.

- **MAC**—Indicates the MAC address of the board.

MAX V Registers

The **MAX V registers** control allows you to view and change the current MAX V register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX V Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the up to three (0-2) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PGM LED (D2-D4) based on the following encoding: ■ 0 = PGM LED (D14) and corresponds to the flash memory page for the factory hardware design ■ 1 = PGM LED (D13) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PGM LED (D12) and corresponds to the flash memory page for the user hardware 2 design

- **PSO**—Sets the MAX V PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX V PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.

- **PSS**—Displays the MAX V PSS register value. Refer to Table 6–1 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values. Refer to Table 6–1 for more information.

Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

This control shows all the devices currently in the JTAG chain. The Cyclone V GT device is always the first device in the chain. The JTAG chain is normally mastered by the On-board USB-Blaster II.

If you plug in an external USB-Blaster cable to the JTAG header (J13), the On-Board USB-Blaster II is disabled.

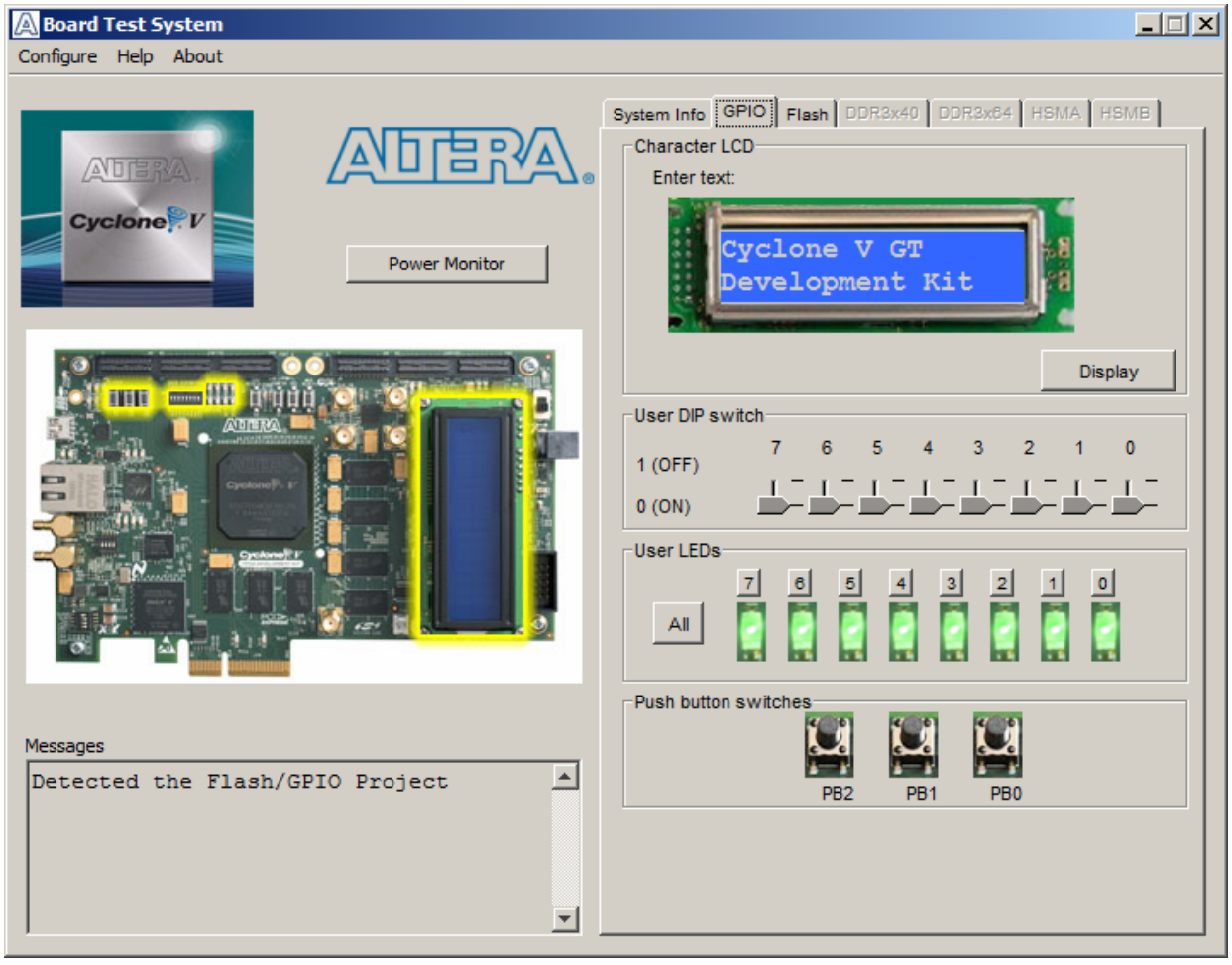
JTAG DIP switch bank (SW3) selects which interfaces are in the chain. Refer to Table 4–1 on page 4–3 for detailed settings.

For details on the JTAG chain, refer to the *Cyclone V GT FPGA Development Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–4 shows the **GPIO** tab.

Figure 6–4. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD and Display

The **Character LCD** controls allow you to type in text strings that appear on the character LCD on your board after clicking **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

Displays the current positions of the switches in the user DIP switch bank. Change the switches on the board to see the graphical display change accordingly.

User LEDs

Displays the current state of the user LEDs. Click the graphical representation of the LEDs to turn the board LEDs on and off. Click **All** to turn on and off all of the user LEDs at once.

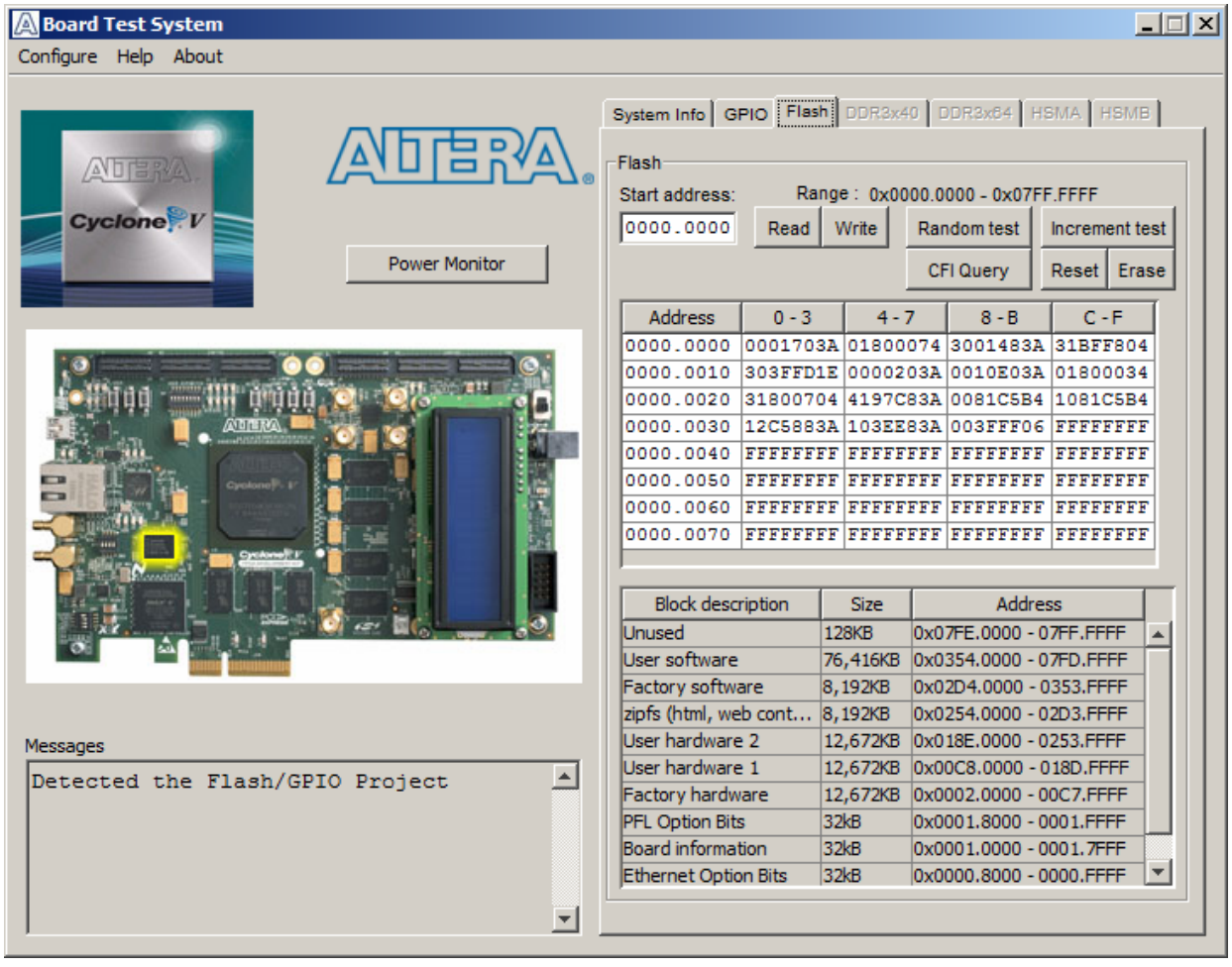
Push Button Switches

Displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6–5 shows the **Flash** tab.

Figure 6–5. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Read and Start Address

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the **Start address** text box and click **Read**. Values starting at the specified address appear in the memory table on the **Flash** tab.

Range

Displays the entire range of the flash memory. If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

Write

Writes the flash memory on your board. To update the flash memory contents:

- Type in values in the memory table cells.
- Press Enter, and click **Write**.

The application writes the new values to flash memory and then reads the values back to guarantee that the memory table accurately reflects the memory contents.

Random Test

Updates the memory table with a random data pattern test. The test area is limited a scratch page in the `Unused` block of flash memory (Table A–1 on page A–1).

CFI Query

Updates the memory table with the CFI ROM table contents from the flash memory.

Increment Test

Updates the memory table with an incrementing data pattern. The test area is limited a scratch page in the `Unused` block of flash memory.

Reset

Starts the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Clears the `Unused` block of flash memory.

Flash Memory Table and Flash Memory Map

The control starting with the **Address** column allows you to write data in each cell. The control underneath is read-only and displays the board's flash memory map.

The DDR3x40 and DDR3x64 Tabs

The **DDR3x40** and **DDR3x64** tabs allow you to read and write the DDR3 memory on your board. Figure 6–6 shows the **DDR3x40** tab.

Figure 6–6. The DDR3x40 Tab

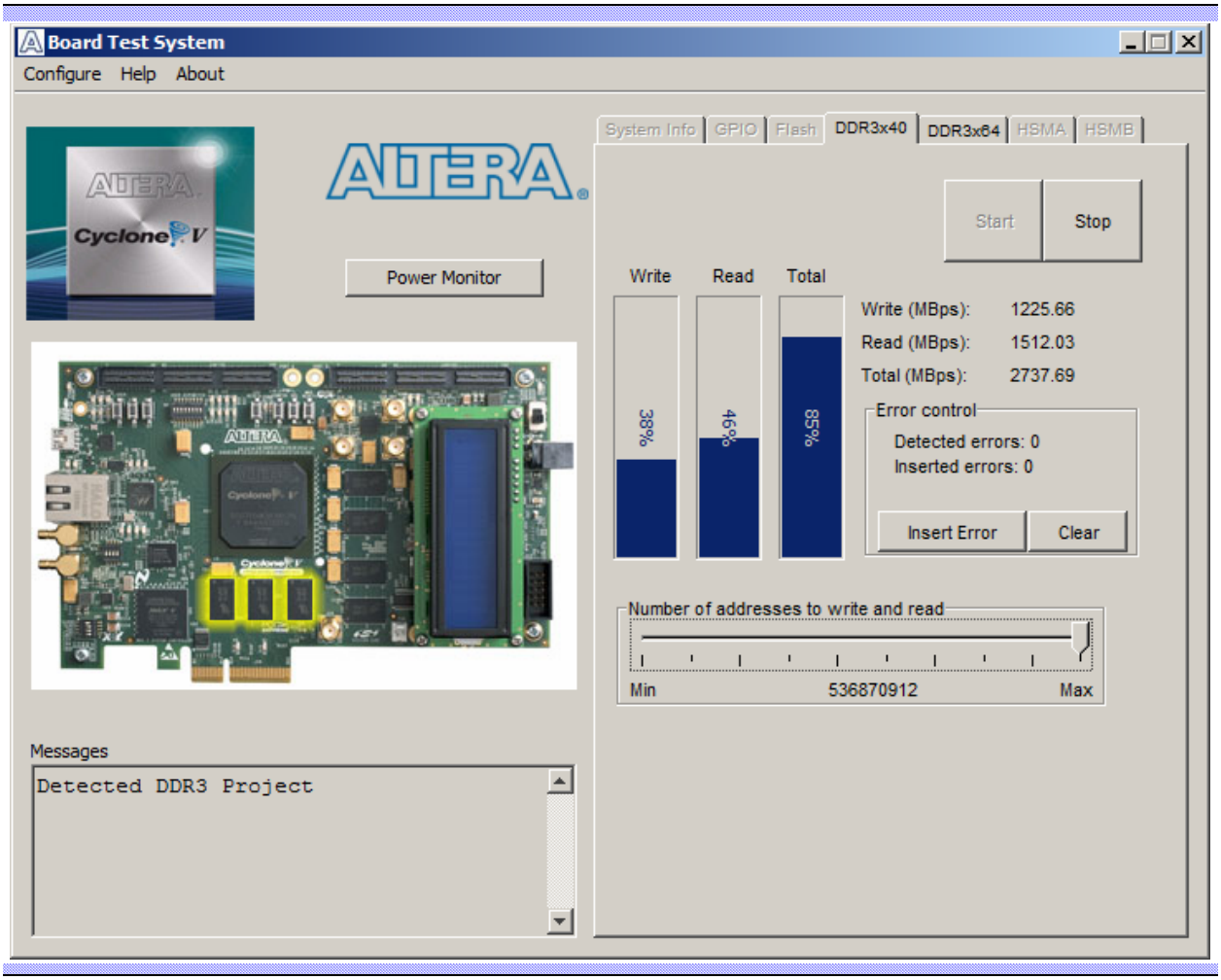
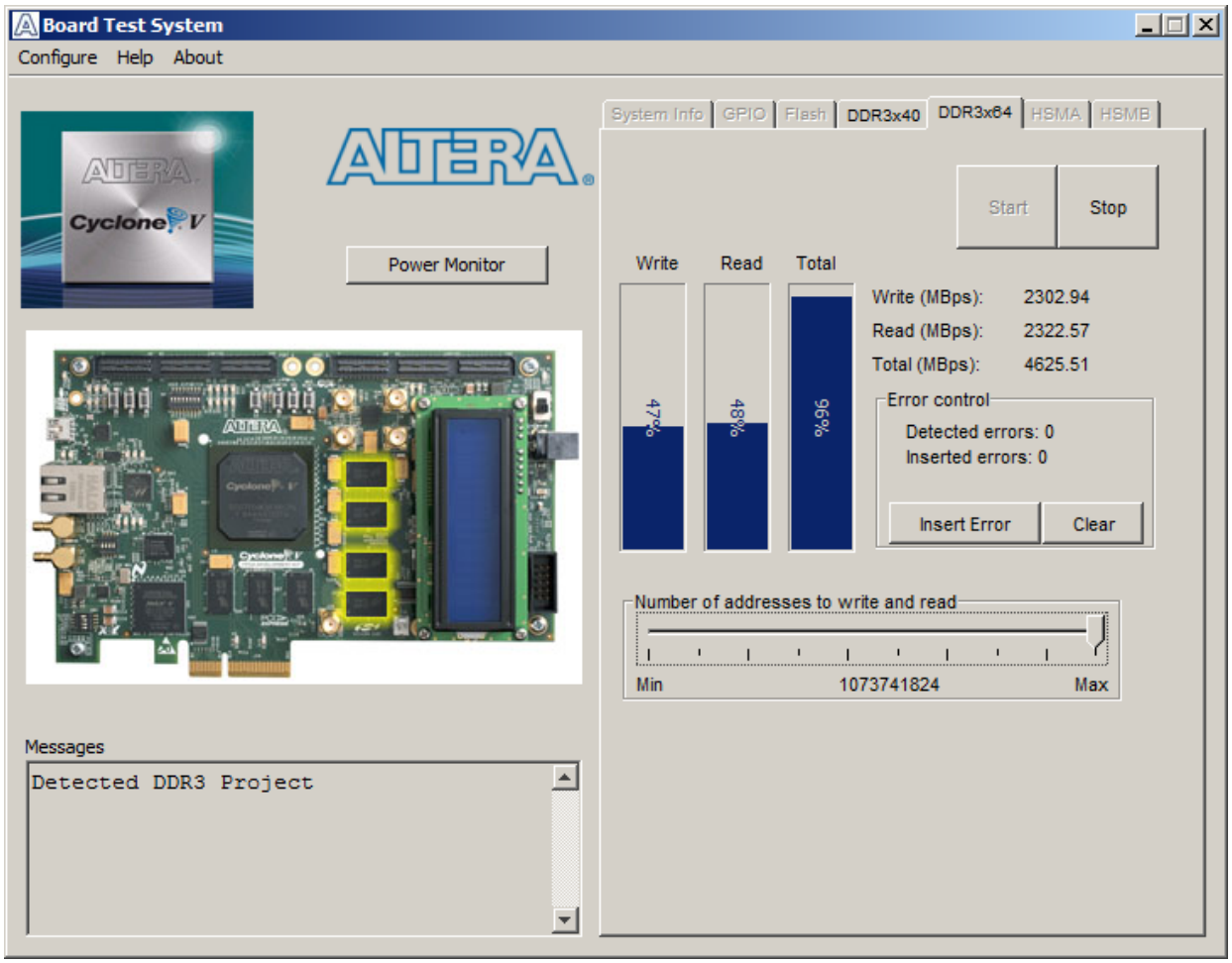


Figure 6–7 shows the **DDR3x64** tab. Except for the tab name and photograph, this tab is identical to the **DDR3x40** tab.

Figure 6–7. The DDR3x64 Tab



The following sections describe the controls on the **DDR3x40** and **DDR3x64** tabs.

Start

Initiates DDR3 memory transaction performance analysis.

Stop

Terminates the transaction performance analysis.

Performance Indicators

Display current transaction performance analysis information collected since you last clicked **Start**:

- **Write**, **Read**, and **Total** performance bars—Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.

- **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**—Show the number of bytes of data analyzed per second.
  - DDR3x40—The theoretical maximum bandwidth is 3200 MBps.
  - DDR3x64—The theoretical maximum bandwidth is 4800 MBps.

Error Control

This group displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

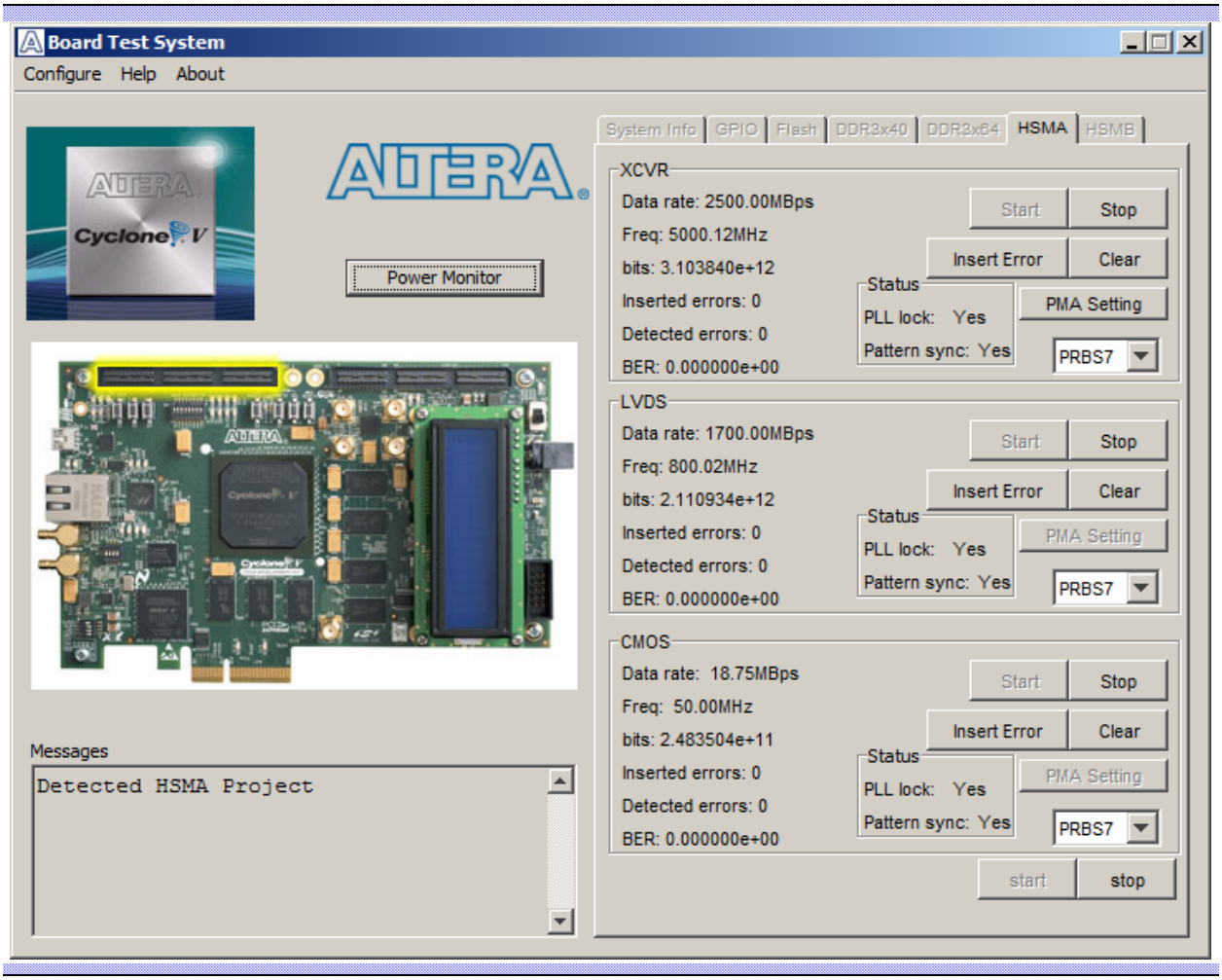
Number of Addresses to Write and Read

This control allows you to determine the number of addresses for each iteration of reads and writes.

The HSMA Tab

The **HSMA** tab (Figure 6–8) allows you to perform loopback tests on the HSMA transceiver (XCVR), HSMA LVDS, and CMOS ports. *HSMA* stands for high-speed mezzanine card for Port A.

Figure 6–8. The HSMA Tab



You must have the loopback HSMA installed on the HSMC Port A connector for this test to work correctly.

The following sections describe the controls on the **HSMA** tab.

Start, Stop

The **Start** and **Stop** controls at the bottom-right of this tab allow you to start and stop testing for all three ports.

XCRV, LVDS, CMOS

The XCRV, LVDS, CMOS groups display the following status information during the loopback test:

Data rate—Displays the current data rate in megabytes per second (MBps).

Freq—Displays the data rate frequency in MHz which is equivalent to MBps.

Bits—Displays the number of bits transmitted since clicking **Start**.

Inserted errors—Displays the number of errors inserted by clicking **Insert Error** button.

Detected errors—Displays the number of bit errors detected by the error checking circuitry.

BER—Displays the bit error rate of the interface.

Status

- **PLL lock**—Displays *Yes* if the PLL is locked.
- **Pattern Sync**—Displays *Yes* if the receiver has detected the input data pattern.

Start— Starts the PRBS data test and begins to monitor and update screen with live test results.

Stop—Stops the PRBS data test.

Insert Error—Inserts an error into a data stream that is detected by the receiver when in loopback mode. With the **Insert Error**, there are differences among the three ports:

- XCVR—Inserts 4 errors at 1 click.
- LVDS—Inserts 3 errors at 1 click.
- CMOS—Inserts 1 error at 1 click.

Clear—Clears the **Detected errors** counter.

PMA Setting—Only available for the XCVR test. This control allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes the selected TX output signal back to the RX input signal on-chip to verify operation without using an external loopback board.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**

  Pre—Not available.

  First post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

  Second post—Not available.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

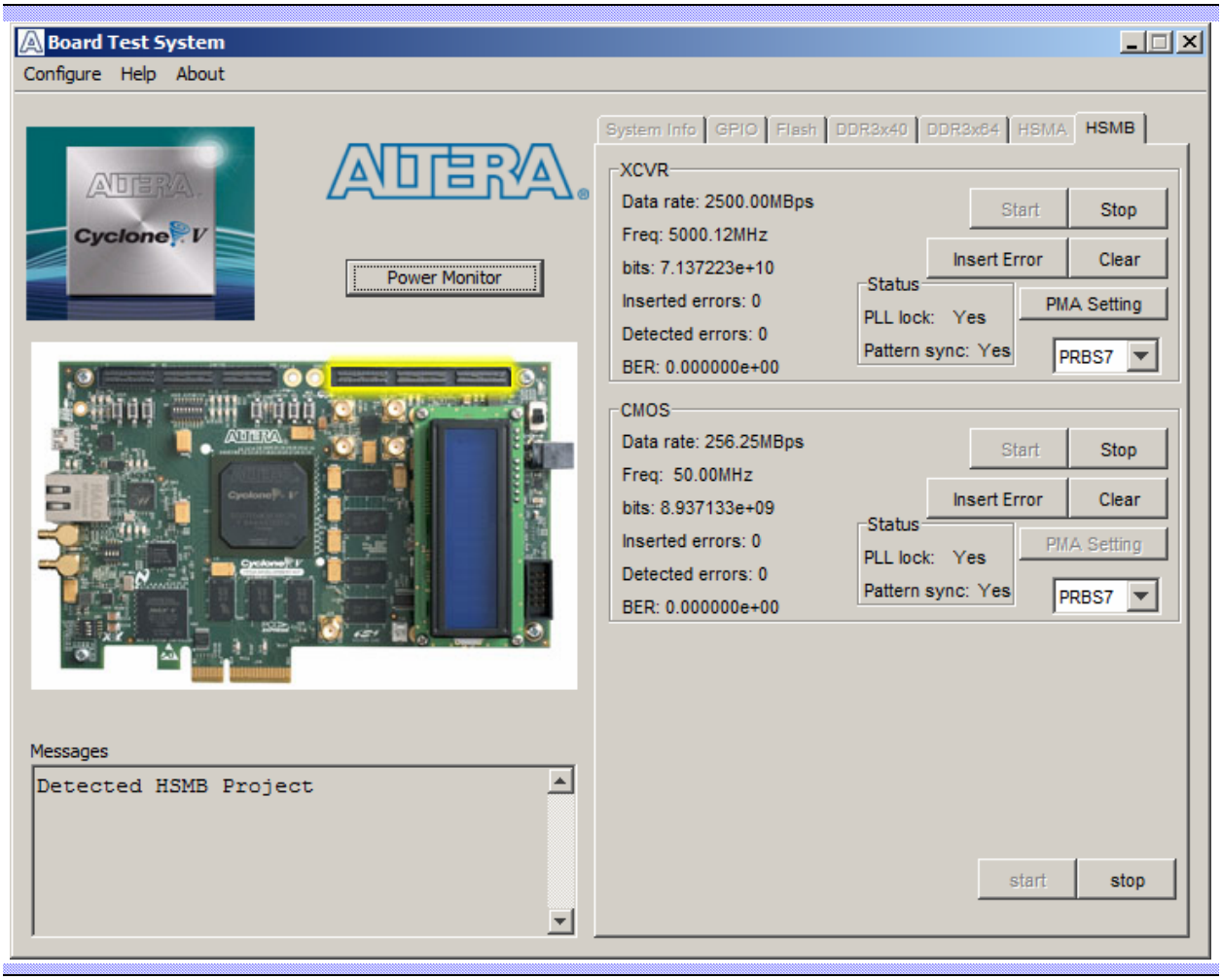
Data Type—Specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Pseudo-random 7-bit sequences
- **PRBS15**—Pseudo-random 15-bit sequences
- **PRBS23**—Pseudo-random 23-bit sequences
- **PRBS31**—Pseudo-random 31-bit sequences
- **HF**—Highest frequency divide-by-4 data pattern `10101010`
- **LF** —Lowest frequency divide-by-4 data pattern `11110000`

The HSMB Tab

The **HSMB** tab (Figure 6–9) allows you to perform loopback tests on the HSMB transceiver (XCVR) and HSMB CMOS ports. *HSMB* stands for high-speed mezzanine card for Port B.

Figure 6–9. The HSMB Tab



You must have the loopback HSMB installed on the HSMC Port B connector for this test to work correctly.

The following sections describe the controls on the **HSMB** tab.

Start, Stop

The **Start** and **Stop** controls at the bottom-right of this tab allow you to start and stop testing for both ports.

XCRV and CMOS

The XCRV and CMOS groups display the following status information during the loopback test:

Data rate—Displays the current data rate in megabytes per second (MBps).

Freq—Displays the data rate frequency in MHz which is equivalent to MBps.

Bits—Displays the number of bits transmitted since clicking **Start**.

Inserted errors—Displays the number of errors inserted by clicking **Insert Error** button.

Detected errors—Displays the number of bit errors detected by the error checking circuitry.

BER—Displays the bit error rate of the interface.

Status

- **PLL lock**—Displays *Yes* if the PLL is locked.
- **Pattern Sync**—Displays *Yes* if the receiver has detected the input data pattern.

Start— Starts the PRBS data test and begins to monitor and update screen with live test results.

Stop—Stops the PRBS data test.

Insert Error—Inserts an error into a data stream that is detected by the receiver when in loopback mode. With the **Insert Error**, there are differences among the three ports:

- XCVR—Inserts 4 errors at 1 click.
- CMOS—Inserts 1 error at 1 click.

Clear—Clears the **Detected errors** counter.

PMA Setting—Only available for the XCVR test. This control allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes the selected TX output signal back to the RX input signal on-chip to verify operation without using an external loopback board.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**

  Pre—Not available.

  First post—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

  Second post—Not available.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type—Specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Pseudo-random 7-bit sequences
- **PRBS15**—Pseudo-random 15-bit sequences
- **PRBS23**—Pseudo-random 23-bit sequences
- **PRBS31**—Pseudo-random 31-bit sequences
- **HF**—Highest frequency divide-by-4 data pattern `10101010`
- **LF** —Lowest frequency divide-by-4 data pattern `11110000`

The Power Monitor

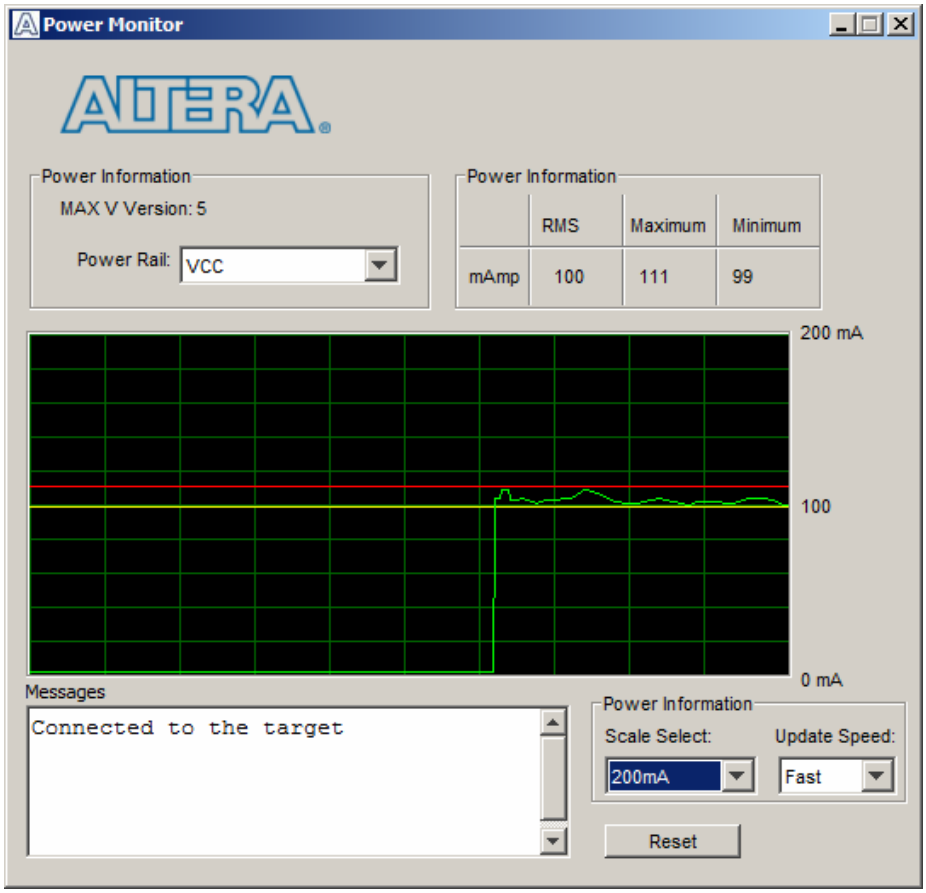
You can start the Power Monitor application with the following:

- The **Power Monitor** button on the Board Test System GUI.
- The **PowerMonitor.exe** application that resides in the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\examples\board_test_system** directory.
- The Windows Start menu: **All Programs > Altera > Cyclone V GT FPGA Development Kit** <*version*> **> Power Monitor**.

Power Monitor Features

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the Cyclone V GT FPGA is consuming. Figure 6–10 shows the Power Monitor.

Figure 6–10. The Power Monitor



Power Monitor Controls

The following sections describe the Power Monitor controls.

General Information

Displays the following information about the MAX V device:

- **MAX V version**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the *<install dir>***kits\cycloneVGT_5cgtfd9ef35_fpga\examples\max5** directories.

Newer revisions of this code might be available on the Cyclone V GT FPGA Development Kit page of the Altera website.

- **Power rail**—Indicates the currently-selected power rail. After selecting the desired rail, click **Reset** to refresh the screen with updated board readings.

  A table with the power rail information is available in the *Cyclone V GT FPGA Development Board Reference Manual*.

Power Information

Displays current, maximum, and minimum numerical power readings in mA.

Power Graph

Displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

Graph Settings

The following controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

Reset

Clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

The Clock Control

You can start the application with the following:

- The **ClockControl.exe** application that resides in the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\examples\board_test_system** directory.
- The Windows Start menu: **All Programs > Altera > Cyclone V GT FPGA Development Kit** <*version*>.

Clock Control Features

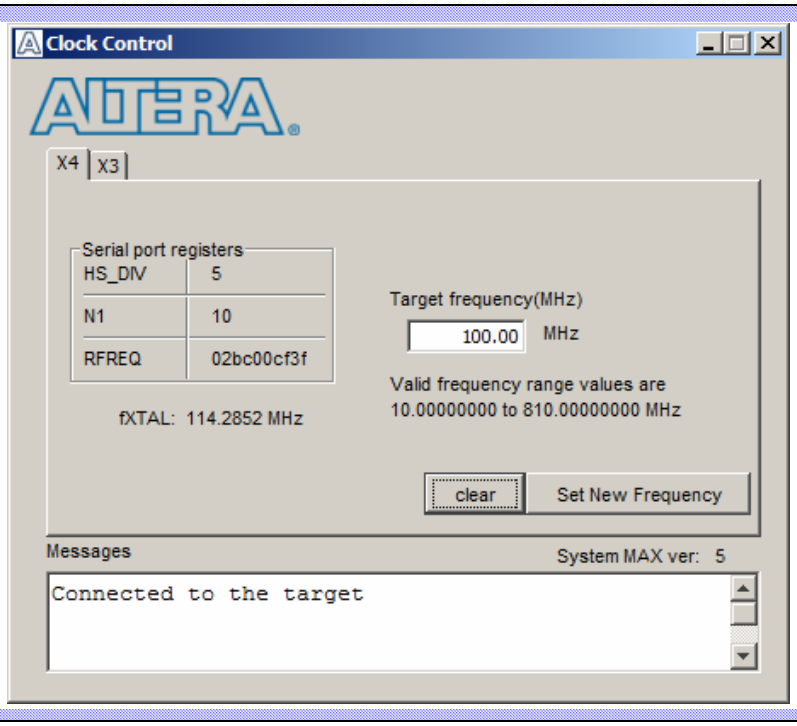
The Clock Control application sets the Si570 and Si571 programmable oscillators to any frequency between 10 MHz and 810 MHz.

- The Si570 (not the Si571) oscillator drives a 1-to-6 buffer that drives a copy of the clock to the following areas of the FPGA:
  - Top, bottom, and right edges
  - REFCLK0 and REFCLK3
- The 6th clock outputs to SMAs J4 and J7 on the board.
- The Clock Control communicates with the MAX V device on the board through the JTAG bus.

- The Si570 and Si571 programmable oscillators are connected to the MAX V device through a 2-wire serial bus.

Figure 6–11 shows the Clock Control **X4** tab (Si570), which has the same controls as the **X3** (Si571) tab.

Figure 6–11. The Clock Control - X4 Tab



Clock Control Controls

The following sections describe the Clock Control controls.

Serial Port Registers

This group shows the current values from the Si570 (**X4** tab) and Si571 (**X3** tab) registers.

For more information about the registers, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

fXTAL

Displays the calculated internal fixed-frequency crystal, based on the serial port register values.

For more information about the f_{XTAL} value and how it is calculated, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

Target Frequency

This control allows you to specify the frequency of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

Clear

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set New Frequency

Sets the programmable oscillator frequency for the selected clock to the value in the **Target frequency** control for the Si570 and Si571 oscillators. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

For more information about the Si570/Si571 and the Cyclone V GT FPGA development board's clocking circuitry and clock input pins, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.

A. Programming the Flash Memory Device

This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device and how to reprogram the user portions of flash memory.

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. The FPGA development board ships with the flash memory preprogrammed with a default factory FPGA configuration. This configuration allows you to run the Board Update Portal design example and the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.

For more information about Altera development tools, refer to the Design Software page of the Altera website.

CFI Flash Memory Map

Table A–1 shows the default memory contents of the 1-Gb CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A–1. Byte Address Flash Memory Map

Block Description	KB Size	Address Range
Unused	128	0x07FE.0000 - 0x07FF.FFFF
User software	76,416	0x0354.0000 - 0x07FD.FFFF
Factory software	8,192	0x02D4.0000 - 0x0353.FFFF
zipfs (html, web content)	8,192	0x0254.0000 - 0x02D3.FFFF
User hardware 2	12,672	0x018E.0000 - 0x0253.FFFF
User hardware 1	12,672	0x00C8.0000 - 0x018D.FFFF
Factory hardware	12,672	0x0002.0000 - 0x00C7.FFFF
PFL option bits	32	0x0001.8000 - 0x0001.FFFF
Board information	32	0x0001.0000 - 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 - 0x0000.FFFF
User design reset vector	32	0x0000.0000 - 0x0000.7FFF

CAUTION

Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to "Restoring the Flash Device to the Factory Settings" on page 4–6.

Preparing Design Files for Flash Programming

The following sections use the following file types:

- Nios II Flash Programmer File (**.flash**)
- Executable and Linking Format File (**.elf**)
- SRAM Object File (**.sof**)
- S-Record File (**.srec**)

You can obtain designs containing prepared **.flash** files from the Cyclone V GT FPGA Development Kit page of the Altera website. You can also create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked **.elf** software design to **.flash**.

For more information about Nios II EDS software tools and practices, refer to the Embedded Software Development page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:
   - For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0xC80000
--pfl --optionbit=0x00018000 --programmingmode=FPP↵
```

   - For Nios II **.elf** files:

```
elf2flash --base=0x00000000 --end=0x0FFFFFFF --reset=0x3540000
--input=<yourfile>_sw.elf --output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec↵
```

The resulting **.flash** files are ready for flash device programming.

The Board Update Portal standard **.flash** format conventionally uses either <*filename*>**_hw.flash** for hardware design files or <*filename*>**_sw.flash** for software design files.

Converting Additional Files

If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format. Once converted, concatenate them into one **.flash** file before using the Board Update Portal to upload them.

After your design files are in the **.flash** format, use one of the following to write the **.flash** files to the user software locations of the flash memory:

- Board Update Portal. Refer to "Using the Board Update Portal to Write User Designs" on page 5–2 for more information.
- Nios II EDS **nios2-flash-programmer** utility.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible **.srec** file to the board using **nios2-flash-programmer**, do the following:

1. Set the SW4.3 DIP switch to the FACT ON (logic 0) to load the Board Update Portal design from flash memory on power up.
2. Attach the USB-Blaster cable and power up the board.
3. If the board has powered up and the LCD displays either *Connecting...* or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the Config Done LED (D7) does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Run the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Restoring the MAX V CPLD to the Factory Settings" on page 4–5 for more information.
5. Click **Add File** and select <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery\c5gt_fpga_bup.sof**.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating that the flash device is ready for programming.
8. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
9. In the Nios II command shell, navigate to the <*install dir*>**\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery** directory.

   You can also navigate to the directory of the **.flash** files you created in "Creating Flash Files Using the Nios II EDS" on page A–2)
10. Type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_hw.flash ↵
```

11. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_sw.flash ↵
```

12. Set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

Programming the board is now complete.

To restore flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page 4–6.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "Using the Board Update Portal to Write User Designs" on page 5–2 for more information.

If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
August 2017	1.2	Added information about programming EPCQ
September 2014	1.1	Additions for CE compliance: CE mark and statements.
December 2013	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.

Visual Cue	Meaning
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
“Subheading Title”	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.

Electromagnetic interference caused by modification of the kit contents is the sole responsibility of the user.

This equipment is designated for use only in an industrial research environment.