Motor Control Application Kit

For XMC1000 Family

KIT_XMC1300_DC_V1

XMC1300 Drive Card V1.0

Board User's Manual

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Microcontroller

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2013-11-05	Initial release

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Introduction

This document describes the features and hardware details of the DriveCard XMC1300 V1 (KIT_XMC1300_DC_V1) designed to work with Infineon's inverter boards. This board is part of Infineon's Motor Control Application Kits.

1 Overview

The drive card KIT_XMC1300_DC_V1 houses the XMC1302 Microcontroller from Infineon Technologies, a power board connector, a set of position interface circuits with hall and encoder connectors, a USIC interface and an isolated on-board debug interface. The board along with a three phase inverter demonstrates the capabilities of the XMC1302. The main use case for this board is to demonstrate the motor control features of the XMC1302 device including tool chain. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The KIT_XMC1300_DC_V1 board is equipped with the following features

- Infineon XMC1302 (ARM® Cortex™-M0-based) Microcontroller, 200 kByte on-chip Flash, TSSOP38
- Connection to power inverter via the power board connector
- Combined hall sensor and encoder interface
- USIC interface connector for connection of UART, SPI or I2C
- 6 LEDs
  - 2 Power indicating LEDs
  - 1 User LED (P0.4)
  - 1 Encoder enable LED
  - 2 Debug LEDs (DEBUG, COM)
- Potentiometer, connected to analog input P2.5 (ADC group 1, channel 7)
- Isolated Debug options
  - On-Board Debugger (SEGGER J-Link LITE) via USB connector
  - Infineon Debug connector 16-pin (0.1") with DriveMonitor USB Stick V2 (KIT_DRIVEMONI_USB_V2)
- Isolated Connectivity
  - UART channel of On-Board Debugger (SEGGER J-Link LITE) via USB connector
- Power supply of MCU domain
  - Via power board connector (5V)
- Power supply of isolated debug domain
  - Via Debug USB connector
  - Via Infineon Debug connector 16-pin

1.2 Block Diagram

Figure 1 shows the functional block diagram of the KIT_XMC1300_DC_V1 board. For more information about the power supply domains please refer to chapter 2.1.

The drive card has got the following building blocks:

- 1 Power Board Connector
- 1 set of position interface connectors (HALL, ENCODER)
- Encoder Enable signals via GPIOs (P0.10)
- 1 User LED connected to GPIOs (P0.4)
- Variable resistor (POTI) connected to GPIO P2.5 (ADC group 1, channel 7)
- USIC0 interface connector (P0.10, P0.14, P1.4, P1.5)
- Isolated On-board Debugger via Debug USB connector (Micro-USB) with UART channel (USIC0, channel 1)
- Optional Infineon Debug interface connector for Drive Monitor USB Stick V2 (KIT_DRIVEMONI_USB_V2)

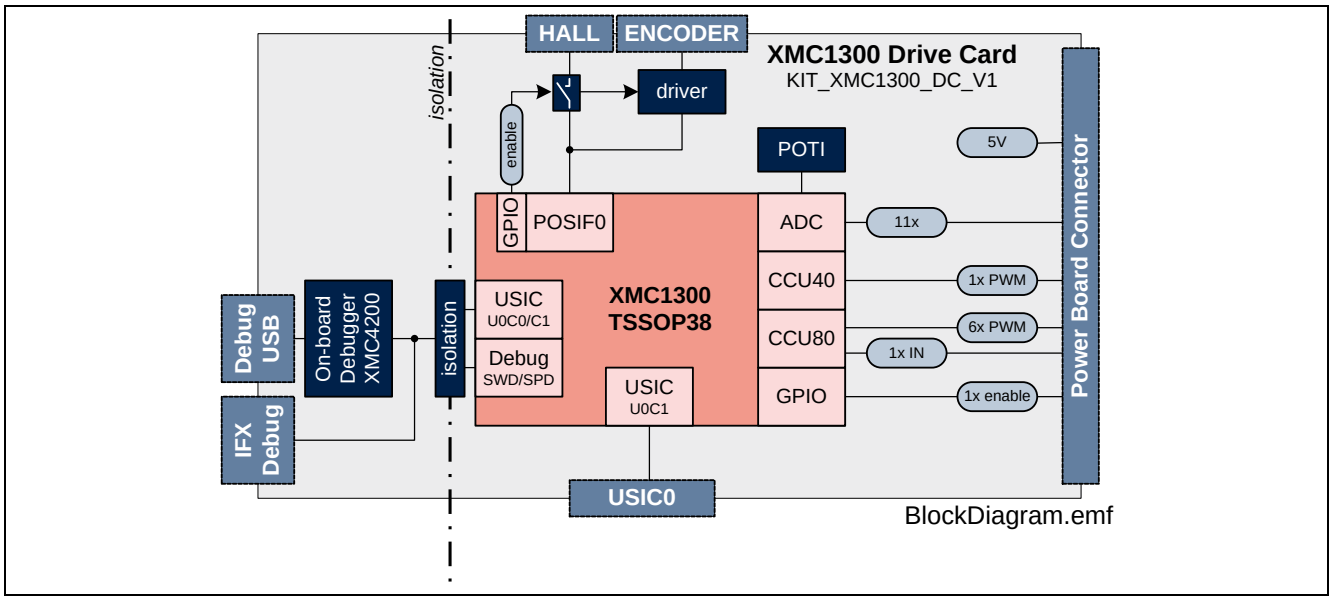


Figure 1 Block Diagram of KIT_XMC1300_DC_V1

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

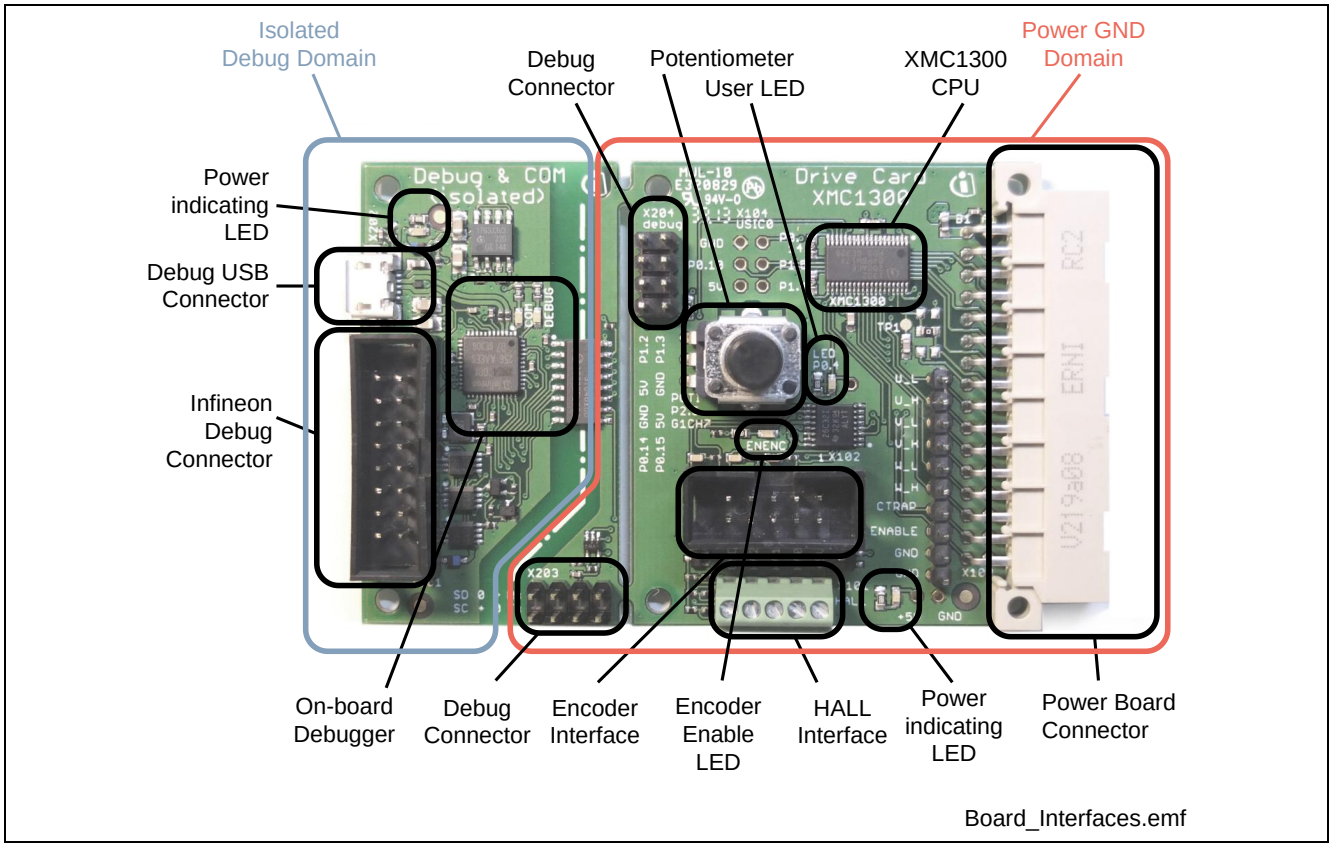


Figure 2 XMC1300 Drive Card (KIT_XMC1300_DC_V1)

2.1 Power Supply

The KIT_XMC1300_DC_V1 board is designed with two galvanically isolated supply domains. On the left side, there is the debug domain, which contains a XMC4200 MCU as on-board debug controller (OBD) as well as level shifters to a 5V debug interface like the drive monitor USB stick (KIT_DRIVEMONI_USB_V2). The debug domain can be powered via the USB plug (5V) as well as the Infineon debug connector.
On the middle to the right side there is the power GND supply domain, which provides the power supply for the MCU and the peripheral components. This supply domain is usually powered from the power board connector. The typical current drawn by the drive card at the power GND domain is about 25 mA.

To indicate the power status of the KIT_XMC1300_DC_V1 board two power indicating LEDs are provided on board (see Figure 3). The LED will be “ON” when the corresponding power rail is powered.

Table 1 Power status LED’s

LED Reference	Power Rail	Voltage	Note
LED101	VDD5	5 V	Power GND domain, must always be “ON”
LED201	VISO5	5 V	Debug supply domain, “ON” if debug domain is intened to be used.

Figure 3 and Figure 4 show details of the power supply concept of the drive card.

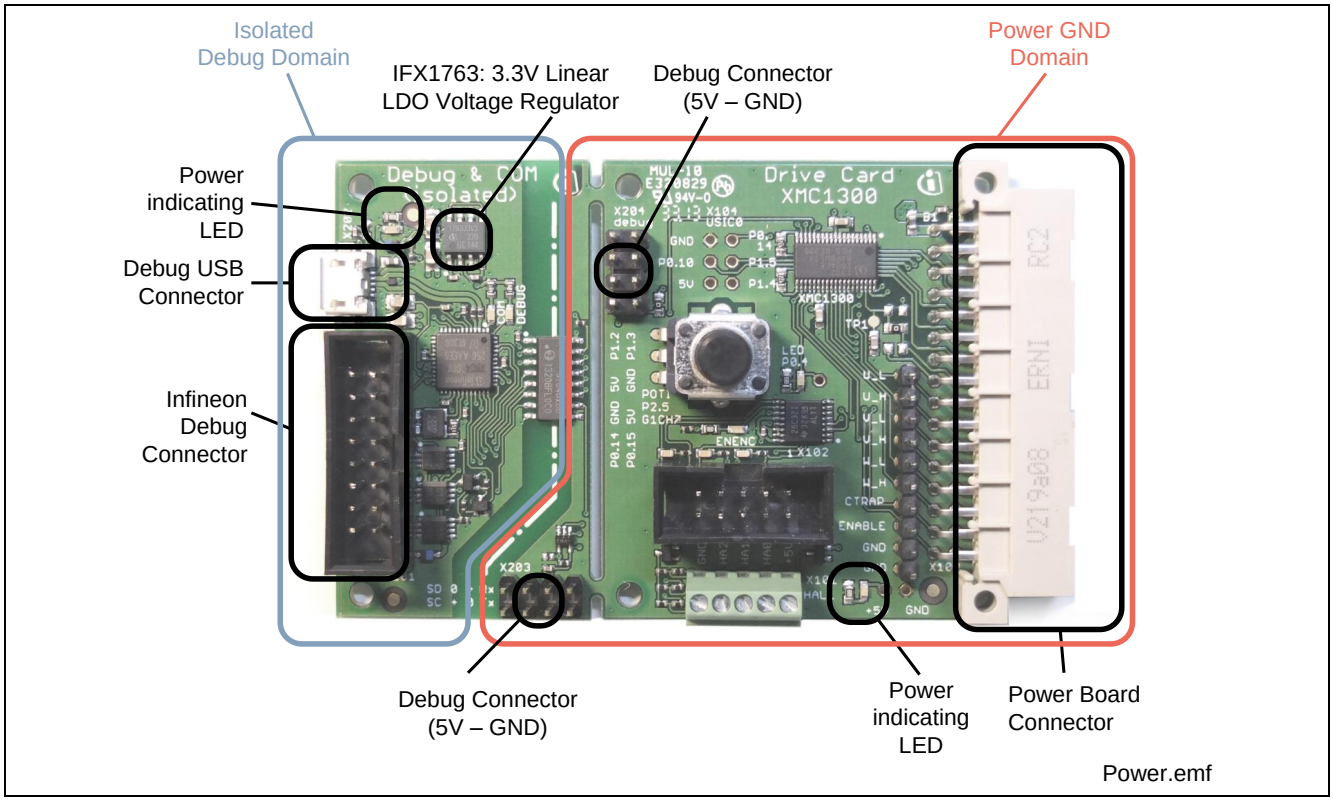


Figure 3 Power Supply Concept and Powering Options

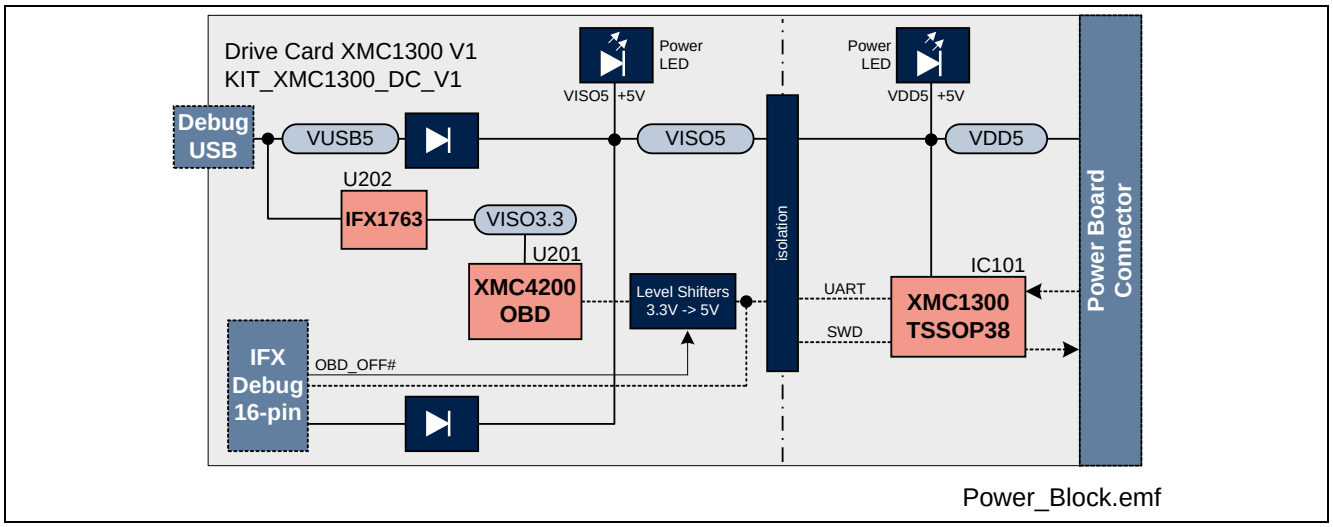


Figure 4 Block Diagram of Power Supply Concept

2.2 Clock Generation

An internal oscillator provides the clock signal to the XMC1300 microcontroller. The CPU can be adjusted to maximum 32MHz (MCLK) whereas the PWM peripherals can be configured to use double of this clock (PCLK).

2.3 Debug Interface

The KIT_XMC1300_DC_V1 is designed to use “Serial Wire Debug” (SWD) or “Single Pin Debug” (SPD) as debug interfaces. It supports debugging via different channels which are all galvanically isolated from the power GND supply domain:

- On-board Debugger
- Infineon Debug Connector (16-pin) with Debug and UART interface

2.3.1 On-board USB Debugger

The on-board debugger [1] supports

- Serial Wire Debug (SWD) [2]
  - SWIO P0.14 (SWD0)
  - SWCLK P0.15 (SWD0)

  or

  - SWIO P1.3 (SWD1)
  - SWCLK P1.2 (SWD1)

- Single Pin Debug (SPD) [2]
  - SPD P0.14 (SPD0)

    or

  - SPD P1.3 (SPD1)

- Full Duplex UART communication via a Virtual COM port
  - PC_RXD P1.2 USIC0CH1.DOUT0
  - PC_TXD P1.3 USIC0CH1.DX0A

    or

  - PC_RXD P0.15 USIC0CH0.DOUT0
  - PC_TXD P0.14 USIC0CH0.DX0A

[1] Attention: The firmware of the on-board debugger requires the latest J-Link driver (V4.62 or higher) and a Serial Port Driver (CDC driver) installed on your computer. Please check “Install J-Link Serial Port Driver” when installing the latest J-Link driver (see Figure 6)

[2] The debug interface type (SPD or SWD) is selected via boot mode index (BMI) configuration. Changing the BMI is supported by the DAVE™ IDE and the “BMI Get Set” window (see Figure 5).

Figure 5 DAVE™ - “BMI Get Set” for XMC1000 Family

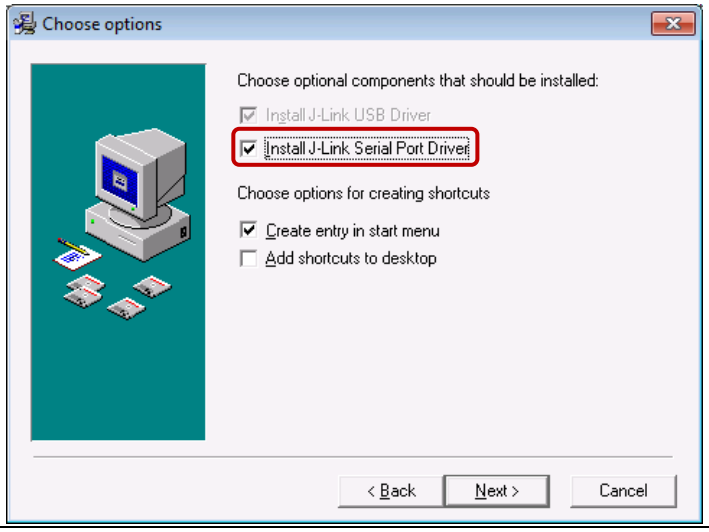


Figure 6 Installation of Serial Port Driver

The on-board debugger can be accessed through the Debug USB connector shown in Figure 7. The Debug LED (LED202) shows the status during debugging.

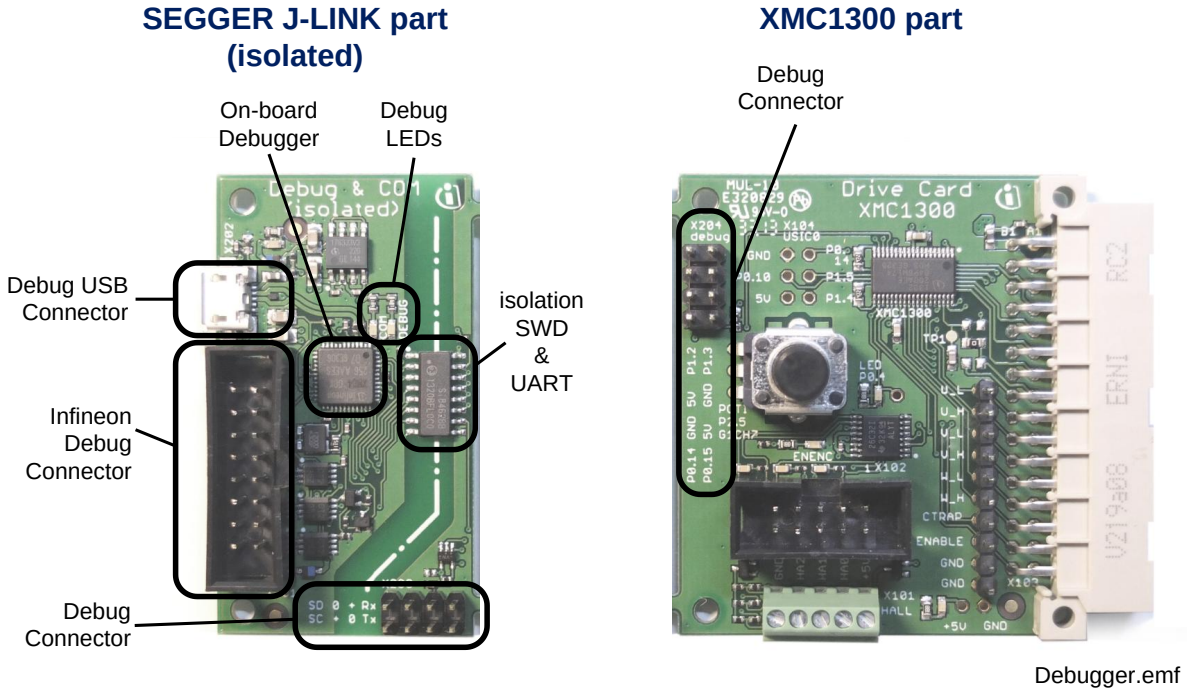


Figure 7 On-Board USB Debugger

When using an external debugger connected to the Infineon Debug Connector (16pin), the on-board debugger has to be switched off. This is done by connecting pin 6 of the Infineon Debug Connector to GNDISO.

2.3.2 Debug Connector (8-pin)

The KIT_XMC1300_DC_V1 board supports debugging via SWD and SPD with the OBD as described in section 2.3.1. The pin assignment is provided in a way that both SWD ports (SWD0 and SWD1) can be selected. Please refer to Figure 8 for details on pin assignment.

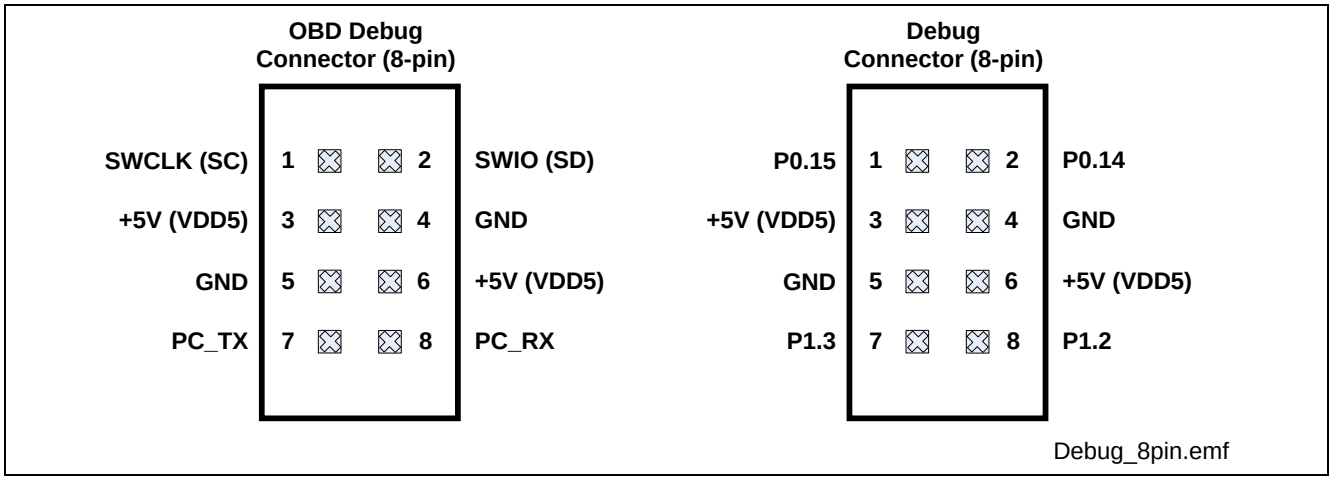


Figure 8 Pin Assignment of Debug Connector (8-pin)

The default connection will provide the following set-up:

- Serial Wire Debug (SWD)
  - SWIO/SPD P0.14 (SWD0)
  - SWCLK P0.15 (SWD0)
- Full Duplex UART communication via a Virtual COM port
  - PC_RXD P1.2 USIC0CH1.DOUT0
  - PC_TXD P1.3 USIC0CH1.DX0A

While breaking off the J-LINK part of the PCB and connecting the debug interface with a ribbon cable, the direct connection will provide the same set-up.

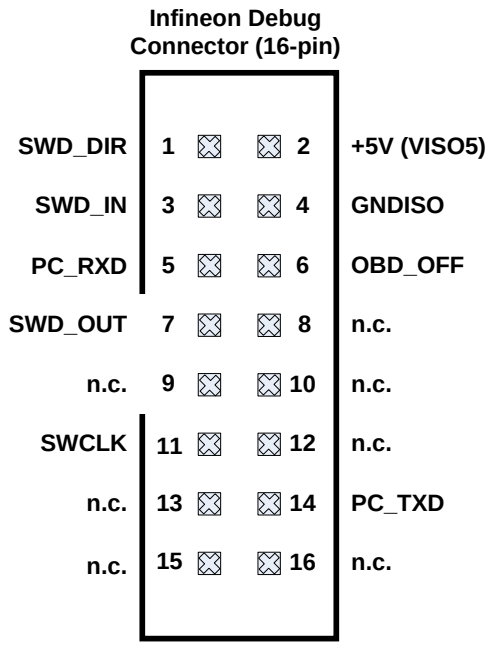
A reverse connection of the debug connector (pin1 to pin8) provides the other set-up:

- Serial Wire Debug (SWD)
  - SWIO/SPD P1.3 (SWD1)
  - SWCLK P1.2 (SWD1)
- Full Duplex UART communication via a Virtual COM port
  - PC_RXD P0.15 USIC0CH0.DOUT0
  - PC_TXD P0.14 USIC0CH0.DX0A

2.3.3 Infineon Debug Connector (16-pin)

The KIT_XMC1300_DC_V1 board supports debugging via Infineon's device access server (DAS), when using KIT_DRIVEMONI_USB_V2 as interface device. The latest release of DAS software can be downloaded from **http://www.infineon.com/das**. When using an external debugger, the on-board debugger (OBD) has to be switched off. This is done by connecting pin 6 to GNDISO. KIT_DRIVEMONI_USB_V2 already provides this connection and the OBD is disabled as soon as the connector is plugged in.

Next to the SWD and SPD debug signals which are provided as unidirectional signals because of the galvanic isolation, UART signals can be accessed through this connector as well. Figure 9 shows the pin assignment of the connector, the following table lists the signals as well.



Infineon_Debug_16pin.emf

Figure 9 Infineon Debug Connector (16-pin)

Pin No.	Signal Name	I/O	Serial Wire Debug
1	SWD_DIR	O	Defines the direction of SWIO
2	+5V (VISO5)	-	+5V supply of isolated debug domain
3	SWD_IN	I	Input signal of SWIO
4	GNDISO	-	Ground of isolated debug domain
5	PC_RXD	I	UART Receive signal (P1.3, DOUT0 USIC0, channel1)
6	OBD_OFF#	I	Disable on-board debug device (Low active)
7	SWD_OUT	O	Output signal of SWIO
8	n.c.	-	Not connected
9	n.c.	-	Not connected
10	n.c.	-	Not connected
11	SWCLK	O	SWD clock signal
12	n.c.	-	Not connected
13	n.c.	-	Not connected
14	PC_TXD	I	UART Transmit signal (P1.2, DX0A, USIC0, channel1)
15	n.c.	-	Not connected
15	n.c.	-	Not connected

2.4 Potentiometer and User LEDs

The KIT_XMC1300_DC_V1 provides a potentiometer which is connected to ADC group1, channel7 and one user LED (P0.4). Next to the LED, a testpoint is available in order to easily connect an oscilloscope's probe for software controlled trigger signals.

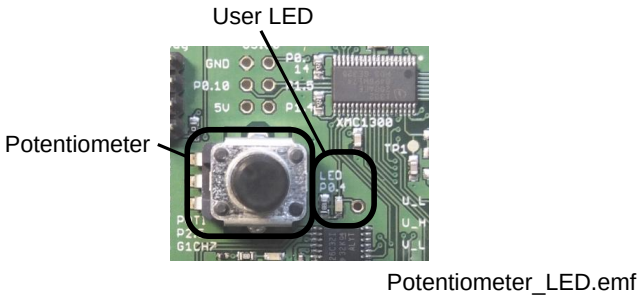


Figure 10 Potentiometer and LEDs

Table 2 Potentiometer

Potentiometer	**Connected to Port Pin**
R103	P2.5 / G1_CH7 (Group 1, channel 7)
User LEDs	**Connected to Port Pin**
LED102	P0.4 (LED)

Attention: The testpoints are referenced to power GND supply domain. Hence they may carry hazzardous voltages.

2.5 USIC0 Connector

The USIC Interface provides access to USIC 0 channel 0, which supports SPI, UART and I2C communication protocolls.

Figure 11 USIC Interface Connector

Table 3 USIC0 Connector X104

Pin	**Port**	**Peripherals**	**Comment**
X104-1	P1.4	USIC0_CH0.DX5E	
X104-2	VDD5	5V	
X104-3	P1.5	USIC0_CH0.DOUT0	
X104-4	P0.10	USIC0_CH0.SELO1 / DX2C	Overlaps with ENENC
X104-5	P0.14	USIC0_CH0.SCLKOUT	Overlaps with SWD0/SPD0
X104-6	GND	GND	

2.6 Hall Sensor and Encoder Connectors

The KIT_XMC1300_DC_V1 provides two pairs of HALL and incremental encoder connectors as indicated in Figure 12. The encoder interface connector provides a differential input which is transformed into single ended signals by an interface IC. The HALL sensor interface provides a pull-up resistor for each HALL sensor signal as well as power supply for the HALL sensors

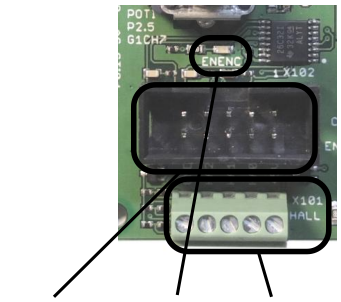


Figure 12 Hall Sensor and Encoder Connectors

Both the HALL and the encoder signals are connected to the same POSIF interface. The ENENC-signal is used to either enable the output signals of the encoder IC or to activate the power supply and pull-up resistor supply of the HALL sensor interface. As a result, both interfaces can be connected at the same time and the user can select by software which interface to use. Figure 13 shows the HALL sensor and encoder interface circuitry. Please refer to Table 4 for details on pin and peripheral assignment.

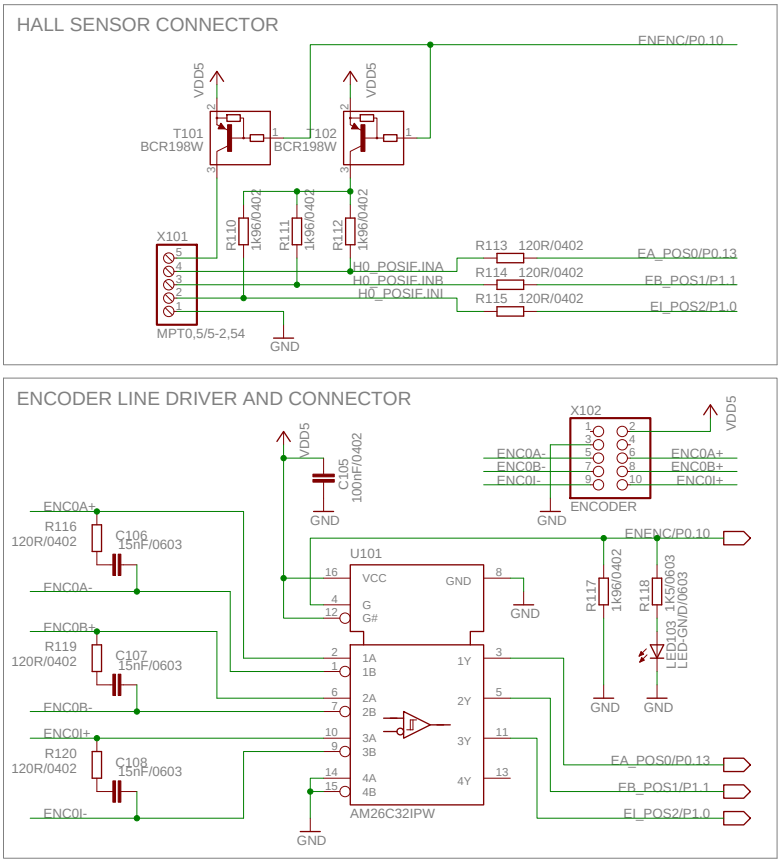


Figure 13 Hall Sensor and Encoder Interface Circuitry

Table 4 HALL Sensor and Encoder Interfaces

Pin	Port	Peripheral
HALL Sensor Interface X101		
1	GND	
2	P1.0	POSIF0.IN2A
3	P1.1	POSIF0.IN1B
4	P0.13	POSIF0.IN0B
5	VDD5	HALL sensor power supply
Encoder Interface X102		
1	n.c.	
2	VDD5	Encoder power supply
3	GND	
4	n.c.	
5	ENCA-	POSIF0.IN0B
6	ENCA+	
7	ENCB-	POSIF0.IN1B
8	ENCB+	
9	ENCI-	POSIF0.IN2A
10	ENCI+	
Enable Encoder		
LED103	P0.10	High: Enable Encoder Interface Low: Enable HALL Interface including supply

2.7 Power Board Connector

The KIT_XMC1300_DC_V1 board provides a power board connector with all the signals required to control the power inverter. Next to the PWM output signals of CCU4 and CCU8 as well as the ADC signals, there are the power supply pins for the power GND domain.

Figure 14 shows a picture of the power board connector. The pin and peripheral assignment can be found in Table 5. In addition, different use cases for three phase inverters can be found in Table 6.

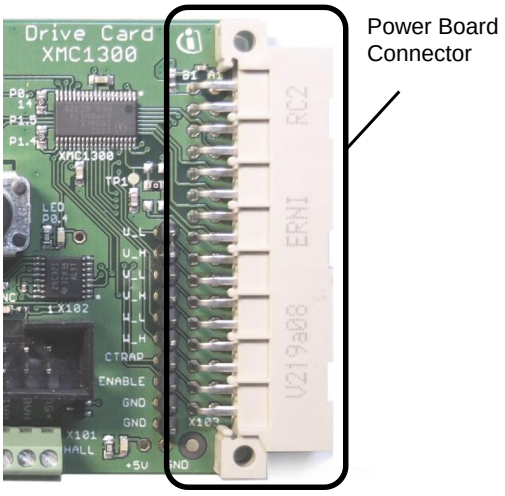


Figure 14 Power Board Connector

Attention: The power board connector is also providing the power supply for the power GND supply domain. Hence it may carry hazzardous voltages.

Table 5 Power Board Connector

X302 MAB32B2	Female FAB32Q2	Function on Power Inverter	Port	Peripherals	
A1	A16	GND	VSS, VSSP		
A2	A15	PFC Gate	P0.5	CCU40.CC40	CMP2.OUT
A3	A14	I_{PFC}	P2.2	VADC0.G0CH7	ACMP2.INN
A4	A13	V_{PFC}	P2.4		VADC0.G1CH6
A5	A12	V_{BEMF_U} / I_U (2)	P2.9	VADC0.G0CH2	VADC0.G1CH4
A6	A11	V_{BEMF_V} / I_V (2)	P2.10	VADC0.G0CH3	VADC0.G1CH2
A7	A10	V_{BEMF_W} / I_W (2)	P2.11	VADC0.G0CH4	VADC0.G1CH3
A8	A9	I_AVG / I_{DClink} (2)	P2.1	VADC0.G0CH6	
A9	A8	U1_L	-		
A10	A7	U1_H	-		
A11	A6	V1_L	-		
A12	A5	V1_H	-		
A13	A4	W1_L	-		
A14	A3	W1_H	-		
A15	A2	CTRAP1	-		
A16	A1	ENPOW1	-		
B1	B16	VCC 5V	VDD, VDDP		
B2	B15	Brake Gate	-		
B3	B14	Brake temp	-		
B4	B13	V_{DClink}	P2.3		VADC0.G1CH5
B5	B12	V_{BEMF_U} / I_U (1)	P2.6	VADC0.G0CH0	
B6	B11	V_{BEMF_V} / I_V (1)	P2.8	VADC0.G0CH1	VADC0.G1CH0
B7	B10	V_{BEMF_W} / I_W (1)	P2.0	VADC0.G0CH5	
B8	B9	I_{DClink} (1)	P2.7		VADC0.G1CH1
B9	B8	U0_L	P0.1	CCU80.OUT01	
B10	B7	U0_H	P0.0	CCU80.OUT00	
B11	B6	V0_L	P0.6	CCU80.OUT11	
B12	B5	V0_H	P0.7	CCU80.OUT10	
B13	B4	W0_L	P0.9 & P0.3	CCU80.OUT21	CCU80.OUT03
B14	B3	W0_H	P0.8 & P0.2	CCU80.OUT20	CCU80.OUT02
B15	B2	CTRAP0	P0.12	CCU80.IN0A,IN1A,IN2A,IN3A	
B16	B1	ENPOW0	P0.11	GPIO	

Note: Please note that the numbering of the power board connector at the drive card is inverse to the numbering at the power board.

Table 6 Use Cases of PWM Signals

X302 (MAB32B2)	Function	Port	Peripheral
2-Level Inverter with CCU80			
B9	U0_L	P0.1	CCU80.OUT01
B10	U0_H	P0.0	CCU80.OUT00
B11	V0_L	P0.6	CCU80.OUT11
B12	V0_H	P0.7	CCU80.OUT10
B13	W0_L	P0.9	CCU80.OUT21
B14	W0_H	P0.8	CCU80.OUT20
B15	CTRAP0	P0.12	CCU80.IN0A,IN1A,IN2A,IN3A
B16	ENPOW0	P0.11	GPIO
2-Level Inverter with CCU80 (2 slices only)			
B9	U0_L	P0.1	CCU80.OUT01
B10	U0_H	P0.0	CCU80.OUT00
B11	V0_L	P0.6	CCU80.OUT11
B12	V0_H	P0.7	CCU80.OUT10
B13	W0_L	P0.3	CCU80.OUT03
B14	W0_H	P0.2	CCU80.OUT02
B15	CTRAP0	P0.12	CCU80.IN0A,IN1A,IN2A,IN3A
B16	Enable0	P0.11	GPIO

3 Production Data

3.1 Schematics

This chapter contains the schematics for the drive card:

- XMC1302 MCU, Power Supply, HALL and Encoder Interface, USIC0 interface
- Isolated On-board Debugger

The board has been designed with Eagle. The full PCB design data of this board can also be downloaded from www.infineon.com/xmc-dev.

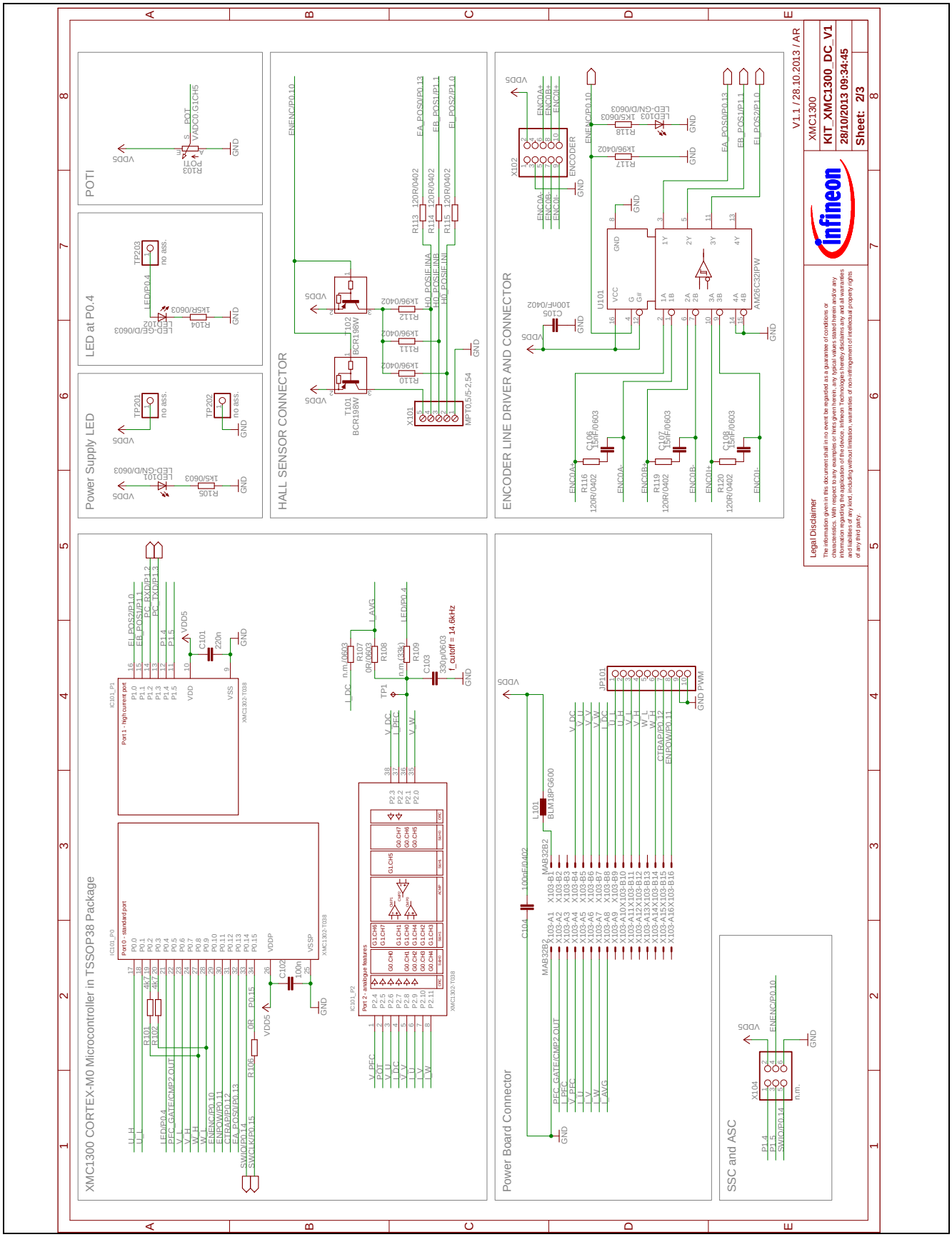


Figure 15 XMC1302 MCU, Power Supply, HALL and Encoder Interface, USIC0 interface

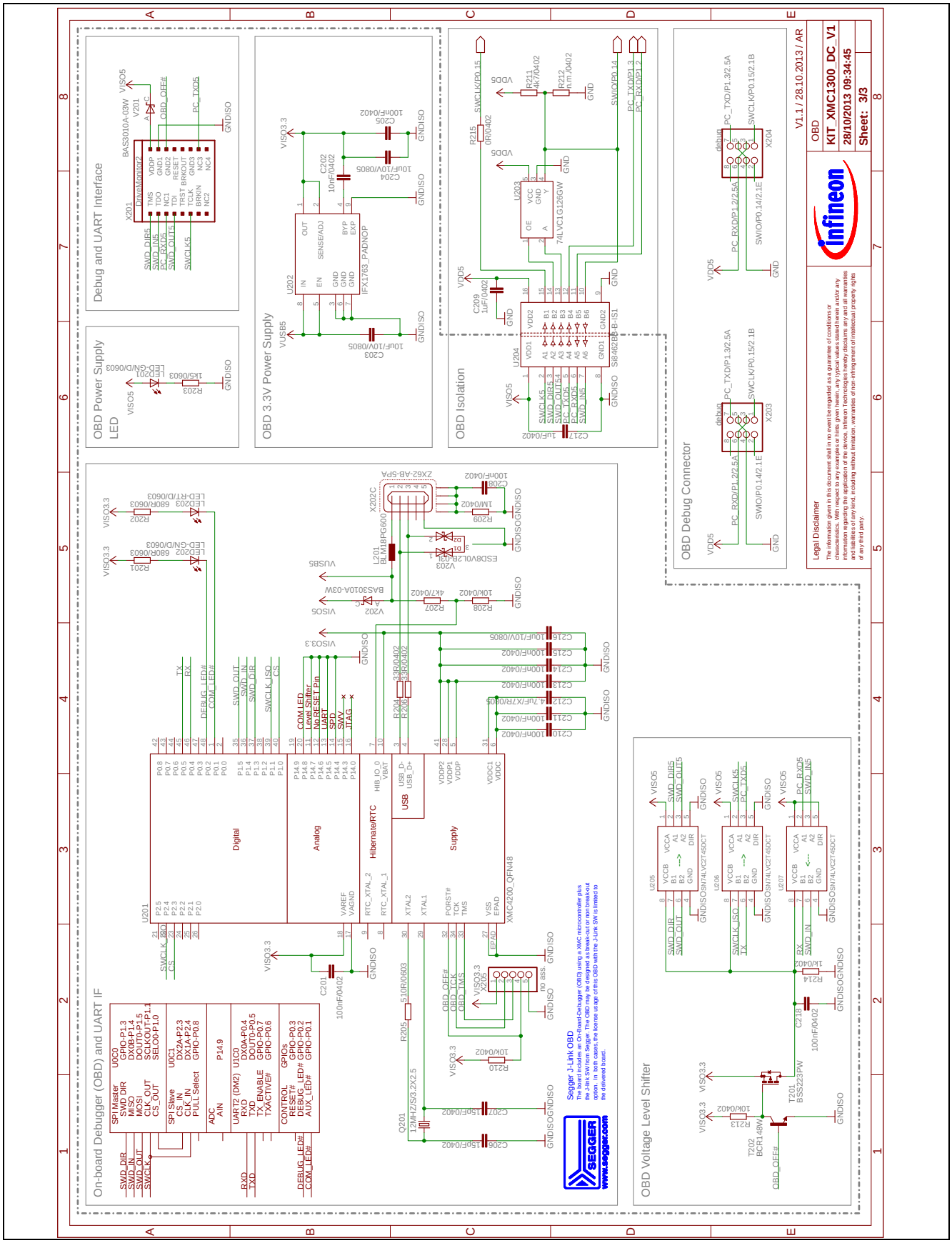


Figure 16 Isolated On-board Debugger

3.2 Component Placement

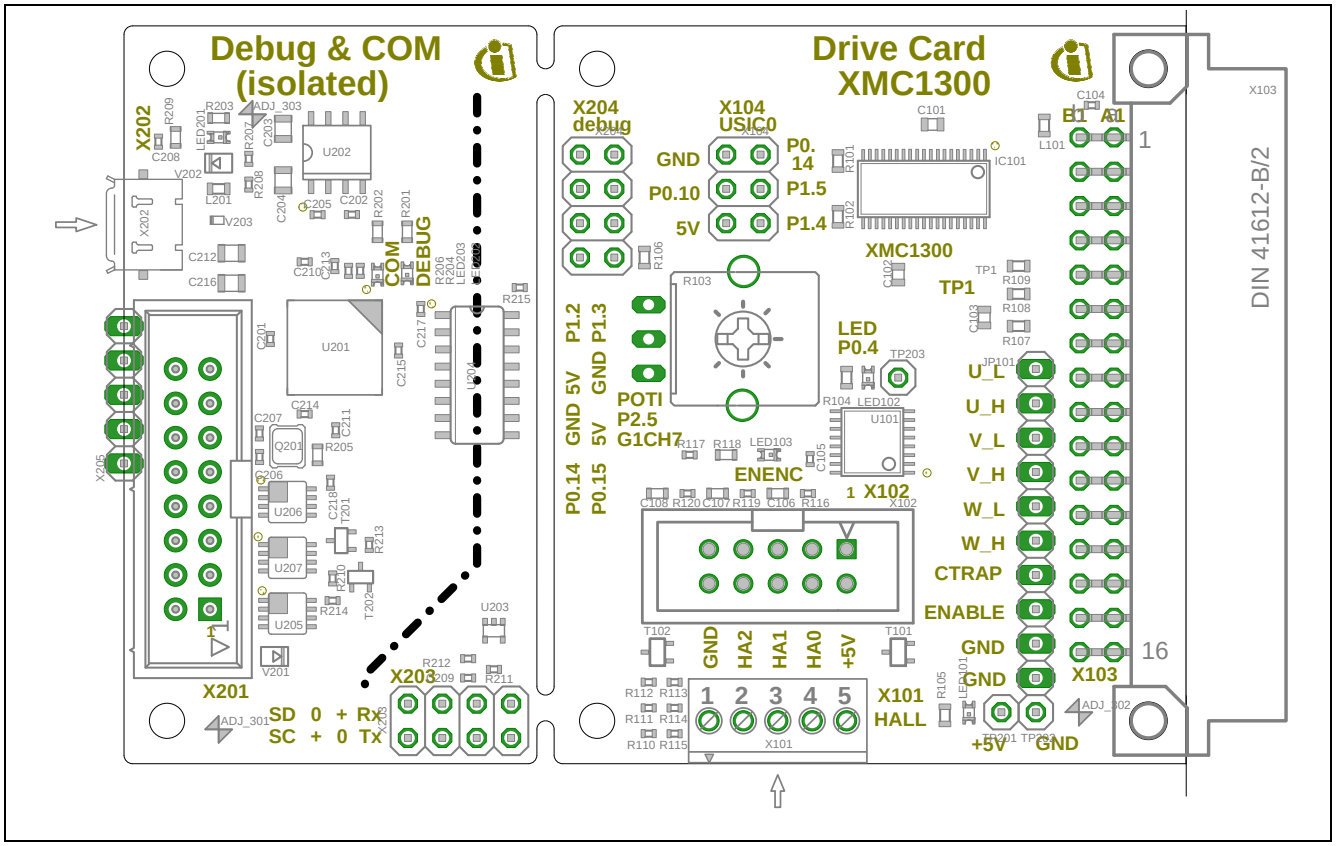


Figure 17 Component Placement

3.3 Bill of Material (BOM)

Table 7 BOM of KIT_XMC1300_DC_V1 Board

Pos. No.	Qty	Value	Device	Reference Des.
1	2	4k7	RESISTOR 0603	R101, R102
2	1	10k	potentiometer	R103
3	1	1k5R/0603	RESISTOR 0603	R104
4	2	1k5/0603	RESISTOR 0603	R105, R203
5	1	0R	RESISTOR 0603	R106
6	1	n.m./0603	RESISTOR 0603	R107
7	1	0R/0603	RESISTOR 0603	R108
8	1	n.m.(33k)	RESISTOR 0603	R109
9	4	1k96/0402	RESISTOR 0402	R110, R111, R112, R117
10	6	120R/0402	RESISTOR 0402	R113, R114, R115, R116, R119, R120
11	1	1K5/0603	RESISTOR 0603	R118
12	2	680R/0603	RESISTOR 0603	R201, R202
13	2	33R/0402	RESISTOR 0402	R204, R206
14	1	510R/0603	RESISTOR 0603	R205
15	2	4k7/0402	RESISTOR 0402	R207, R211
16	3	10k/0402	RESISTOR 0402	R208, R210, R213
17	1	1M/0402	RESISTOR 0603	R209
18	1	n.m./0402	RESISTOR 0402	R212
19	1	1k/0402	RESISTOR 0402	R214
20	1	0R/0402	RESISTOR 0402	R215
21	1	220n	CAPACITOR 0603	C101
22	1	100n	CAPACITOR 0603	C102
23	1	330p/0603	CAPACITOR 0603	C103
24	11	100nF/0402	CAPACITOR 0402	C104, C105, C201, C205, C208, C210, C211, C213, C214, C215, C218
25	3	15nF/0603	CAPACITOR 0603	C106, C107, C108
26	1	10nF/0402	CAPACITOR 0402	C202
27	3	10uF/10V/0805	CAPACITOR 0805K	C203, C204, C216
28	2	15pF/0402	CAPACITOR 0402	C206, C207
29	2	1uF/0402	CAPACITOR 0402	C209, C217
30	1	4.7uF/X7R/0805	CAPACITOR 0805K	C212
31	2	12MHZ/S/3.2X2.5	CRYSTAL	Q201
32	2	BLM18PG600	FERRIT BEAD	L101, L201
33	4	LED-GN/D/0603	LEDCHIPLED 0603	LED101, LED103, LED201, LED202
34	1	LED-GE/D/0603	LEDCHIPLED 0603	LED102
35	1	LED-RT/D/0603	LEDCHIPLED 0603	LED203
36	2	BCR198W	TRANSISTOR	T101, T102
37	1	BSS223PW	TRANSISTOR	T201
38	1	BCR148W	TRANSISTOR	T202
39	1	XMC1302_TSSOP38	INFINEON MCU	IC101
40	1	IFX1763	INFINEON LDO	U202
41	1	AM26C32IPW	ENCODER IC	U101
42	1	XMC4200_QFN48	INFINEON MCU	U201

43	1	Si8462BB-B-IS1	ISOLATED DIGITAL	U204
44	1	74LVC1G126GW	LOGIC	U203
45	3	SN74LVC2T45DCT	LOGIC	U205, U206, U207
46	2	BAS3010A-03W	BAT60	V201, V202
47	1	ESD8V0L2B-03L	ESD DIODE	V203
48	1	ZX62-AB-5PA	MICRO-USB	X202
49	1	W1*10	CONNECTOR	JP101
50	1	CONP_2X05	CONNECTOR	X102
51	1	MAB32B2	CONNECTOR	X103
52	1	MPT0,5/5-2,54	CONNECTOR	X101
53	2	W2*4	CONNECTOR (DEBUG)	X203, X204
54	1	W2*3	CONNECTOR (USIC)	X104

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